



H61H2-AM

Rev :
1.1.

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22	LAN PHY - 82579, USBLAN
23	AUDIO ALC662-VC
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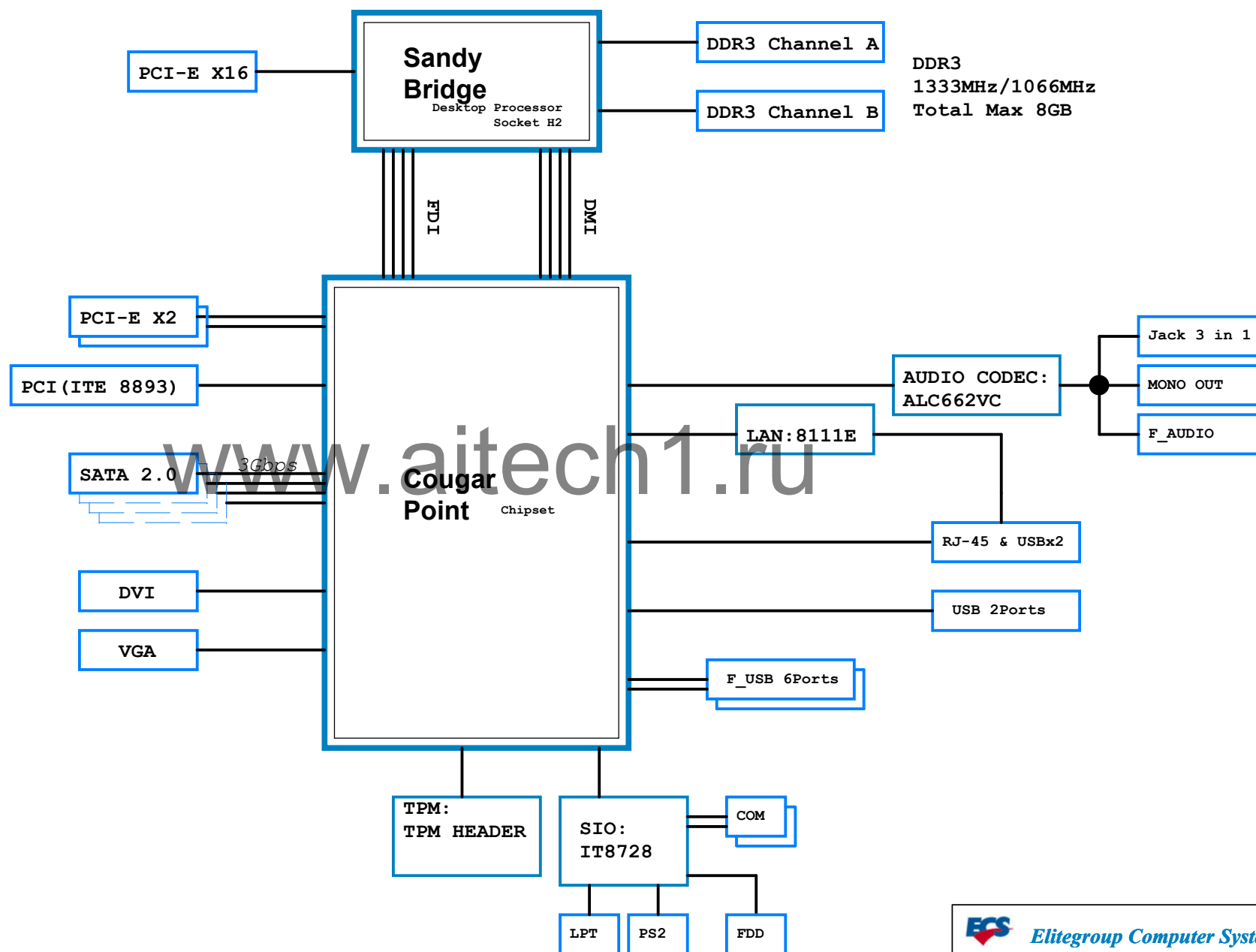
NOTE:

Design by
428971Sugar Bay and Bromolow-WS Platforms - Design Guide - Rev. 1.0,
428880_428880_Cougar_Point_Desktop_Ballout_Mech_Package_Rev1p0.zip

REVISION HISTORY:

Rev	Date	Notes
V.A	2010/04/19	Initial version
V.B	2010/09/13	
V.1.0	2010/09/30	
V.1.9	2010/12/22	

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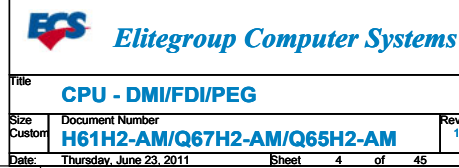
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO1	VCC3	OBR	GPI
GPIO12	3VSB	LAN_DISABLE_L	Native
GPIO13	3VSB	LPC_PME_L	GPI
GPIO23	VCC3	HDPANEL_DETECT	Native
GPIO24	3VSB	PCH_SKTOCC_L	GPO
GPIO27	SB_3VSB	DEEP LANWAKEB	GPI
GPIO45	3VSB	SPI_WPSW	Native
GPIO59	3VSB	LAN_LED_D	Native
GPIO72	3VSB	SPI_WP0_L	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO16		SIO_BEEP	
GPIO22		SIO_LED1	
GPIO23		SIO_LED0	

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9 M_DATA_A[0..63]	← M_DATA A[0..63]
9 M_DQS_A_P[0..7]	← M_DQS A P[0..7]
9 M_DQS_A_N[0..7]	← M_DQS A N[0..7]
9 M_MA_A[0..15]	← M_MA A[0..15]
9 M_BS_A[0..2]	← M_BS A[0..2]
9 M_CS_A_L[0..3]	← M_CS A L[0..3]
9 M_CKE_A[0..3]	← M_CKE A[0..3]
9 M_ODT_A[0..3]	← M_ODT A[0..3]
9 M_CLK_A_P[0..3]	← M_CLK A P[0..3]
9 M_CLK_A_N[0..3]	← M_CLK A N[0..3]
9 M_WE_A_L	← M_WE A L
9 M_CAS_A_L	← M_CAS A L
9 M_RAS_A_L	← M_RAS A L

DDR3 CH.A

9,10 DDR3_DRAMRST_L ← DDR3_DRAMRST_L

10 M_DATA_B[0..63]	← M_DATA B[0..63]
10 M_DQS_B_P[0..7]	← M_DQS B P[0..7]
10 M_DQS_B_N[0..7]	← M_DQS B N[0..7]
10 M_MA_B[0..15]	← M_MA B[0..15]
10 M_BS_B[0..2]	← M_BS B[0..2]
10 M_CS_B_L[0..3]	← M_CS B L[0..3]
10 M_CKE_B[0..3]	← M_CKE B[0..3]
10 M_ODT_B[0..3]	← M_ODT B[0..3]
10 M_CLK_B_P[0..3]	← M_CLK B P[0..3]
10 M_CLK_B_N[0..3]	← M_CLK B N[0..3]
10 M_WE_B_L	← M_WE B L
10 M_CAS_B_L	← M_CAS B L
10 M_RAS_B_L	← M_RAS B L

DDR3 CH.B

M_DATA_A0	AJ3	SA_DQ_0
M_DATA_A1	AJ4	SA_DQ_1
M_DATA_A2	AL3	SA_DQ_2
M_DATA_A3	AL4	SA_DQ_3
M_DATA_A4	AJ2	SA_DQ_4
M_DATA_A5	AJ1	SA_DQ_5
M_DATA_A6	AL2	SA_DQ_6
M_DATA_A7	AL1	SA_DQ_7
M_DATA_A8	AN1	SA_DQ_8
M_DATA_A9	AN4	SA_DQ_9
M_DATA_A10	AR3	SA_DQ_10
M_DATA_A11	AR4	SA_DQ_11
M_DATA_A12	AR2	SA_DQ_12
M_DATA_A13	AN3	SA_DQ_13
M_DATA_A14	AR2	SA_DQ_14
M_DATA_A15	AR1	SA_DQ_15
M_DATA_A16	AV2	SA_DQ_16
M_DATA_A17	AV3	SA_DQ_17
M_DATA_A18	AV5	SA_DQ_18
M_DATA_A19	AW5	SA_DQ_19
M_DATA_A20	AU2	SA_DQ_20
M_DATA_A21	AU3	SA_DQ_21
M_DATA_A22	AU5	SA_DQ_22
M_DATA_A23	AV6	SA_DQ_23
M_DATA_A24	AY7	SA_DQ_24
M_DATA_A25	AU7	SA_DQ_25
M_DATA_A26	AV9	SA_DQ_26
M_DATA_A27	AU9	SA_DQ_27
M_DATA_A28	AV7	SA_DQ_28
M_DATA_A29	AW7	SA_DQ_29
M_DATA_A30	AW9	SA_DQ_30
M_DATA_A31	AY9	SA_DQ_31
M_DATA_A32	AU35	SA_DQ_32
M_DATA_A33	AW37	SA_DQ_33
M_DATA_A34	AU39	SA_DQ_34
M_DATA_A35	AU36	SA_DQ_35
M_DATA_A36	AW35	SA_DQ_36
M_DATA_A37	AY36	SA_DQ_37
M_DATA_A38	AU38	SA_DQ_38
M_DATA_A39	AU37	SA_DQ_39
M_DATA_A40	AR40	SA_DQ_40
M_DATA_A41	AR37	SA_DQ_41
M_DATA_A42	AN38	SA_DQ_42
M_DATA_A43	AN37	SA_DQ_43
M_DATA_A44	AR39	SA_DQ_44
M_DATA_A45	AR38	SA_DQ_45
M_DATA_A46	AN39	SA_DQ_46
M_DATA_A47	AN40	SA_DQ_47
M_DATA_A48	AL40	SA_DQ_48
M_DATA_A49	AL37	SA_DQ_49
M_DATA_A50	AJ38	SA_DQ_50
M_DATA_A51	AJ37	SA_DQ_51
M_DATA_A52	AL38	SA_DQ_52
M_DATA_A53	AL38	SA_DQ_53
M_DATA_A54	AJ40	SA_DQ_54
M_DATA_A55	AJ40	SA_DQ_55
M_DATA_A56	AG40	SA_DQ_56
M_DATA_A57	AG37	SA_DQ_57
M_DATA_A58	AE38	SA_DQ_58
M_DATA_A59	AE37	SA_DQ_59
M_DATA_A60	AG39	SA_DQ_60
M_DATA_A61	AG38	SA_DQ_61
M_DATA_A62	AE39	SA_DQ_62
M_DATA_A63	AE40	SA_DQ_63

M_DQS_A_P0	AK3	SA_DQS_0
M_DQS_A_P1	AP3	SA_DQS_1
M_DQS_A_P2	AW4	SA_DQS_2
M_DQS_A_P3	AV8	SA_DQS_3
M_DQS_A_P4	AV37	SA_DQS_4
M_DQS_A_P5	AP38	SA_DQS_5
M_DQS_A_P6	AK38	SA_DQS_6
M_DQS_A_P7	AF38	SA_DQS_7

M_DQS_A_N0	AK2	SA_DQS#_0
M_DQS_A_N1	AP2	SA_DQS#_1
M_DQS_A_N2	AV4	SA_DQS#_2
M_DQS_A_N3	AV8	SA_DQS#_3
M_DQS_A_N4	AV36	SA_DQS#_4
M_DQS_A_N5	AP39	SA_DQS#_5
M_DQS_A_N6	AK39	SA_DQS#_6
M_DQS_A_N7	AF39	SA_DQS#_7

BALLMAP_REV=1.4

SA_WE#
SA_CAS#
SA_RAS#

SA_BS_0
SA_BS_1
SA_BS_2

SA_CS#_0
SA_CS#_1
SA_CS#_2
SA_CS#_3

SA_CKE_0
SA_CKE_1
SA_CKE_2
SA_CKE_3

SA_ODT_0
SA_ODT_1
SA_ODT_2
SA_ODT_3

SA_CK_0
SA_CK#_0
SA_CK_1
SA_CK#_1
SA_CK_2
SA_CK#_2
SA_CK_3
SA_CK#_3

SM_DRAMRST#

SA_DQS_8
SA_DQS#_8

SA_ECC_CB_0
SA_ECC_CB_1
SA_ECC_CB_2
SA_ECC_CB_3
SA_ECC_CB_4
SA_ECC_CB_5
SA_ECC_CB_6
SA_ECC_CB_7

DDR_0

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SKT_H2_CRB

DDR3 CH.A

AV27	M_MA_A0
AV24	M_MA_A1
AW24	M_MA_A2
AW23	M_MA_A3
AV23	M_MA_A4
AT24	M_MA_A5
M_DATA_B6	AJ6
AU22	M_MA_A7
AV22	M_MA_A8
AT22	M_MA_A9
AV28	M_MA_A10
AU21	M_MA_A11
AT21	M_MA_A12
AW32	M_MA_A13
AU20	M_MA_A14
SA_MA_14	SA_MA_14
SA_MA_15	SA_MA_15

AW29 M_WE_A_L
AV30 M_CAS_A_L
AU28 M_RAS_A_L

AV29 M_BS_A0
AW28 M_BS_A1
AV20 M_BS_A2

AU29 M_CS_A_L0
AV32 M_CS_A_L1
AW30 M_CS_A_L2
AU33 M_CS_A_L3

AV19 M_CKE_A0
AT19 M_CKE_A1
AU18 M_CKE_A2
AV18 M_CKE_A3

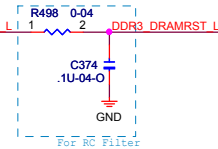
AV31 M_ODT_A0
AU32 M_ODT_A1
AU30 M_ODT_A2
AW33 M_ODT_A3

AY25 M_CLK_A_P0
AW25 M_CLK_A_N0
AU24 M_CLK_A_P1
AU25 M_CLK_A_N1
AW27 M_CLK_A_P2
AY27 M_CLK_A_N2
AV26 M_CLK_A_P3
AW26 M_CLK_A_N3

AW18DDR3_DRAMRST_R_L

AV13
AV12

AU12
AU14
AU13
AY13
AU15
AU11
AY12
AW12



Desktop dosen't support ECC

Pay Attention to This Part!

M_DATA_B0	AG7	SB_DQ_0
M_DATA_B1	AG8	SB_DQ_1
M_DATA_B2	AJ9	SB_DQ_2
M_DATA_B3	AJ8	SB_DQ_3
M_DATA_B4	AG5	SB_DQ_4
M_DATA_B5	AG6	SB_DQ_5
M_DATA_B6	AJ6	SB_DQ_6
M_DATA_B7	AJ7	SB_DQ_7
M_DATA_B13	AL7	SB_DQ_8
M_DATA_B9	AM7	SB_DQ_9
M_DATA_B11	AM10	SB_DQ_10
M_DATA_B15	AL10	SB_DQ_11
M_DATA_B12	AL6	SB_DQ_12
M_DATA_B8	AM6	SB_DQ_13
M_DATA_B14	AL9	SB_DQ_14
M_DATA_B10	AM9	SB_DQ_15
M_DATA_B16	AP7	SB_DQ_16
M_DATA_B17	AP7	SB_DQ_17
M_DATA_B18	AP10	SB_DQ_18
M_DATA_B19	AR10	SB_DQ_19
M_DATA_B20	AP6	SB_DQ_20
M_DATA_B21	AR6	SB_DQ_21
M_DATA_B22	AP9	SB_DQ_22
M_DATA_B23	AP9	SB_DQ_23
M_DATA_B24	AM12	SB_DQ_24
M_DATA_B25	AM13	SB_DQ_25
M_DATA_B26	AR13	SB_DQ_26
M_DATA_B27	AP13	SB_DQ_27
M_DATA_B28	AL12	SB_DQ_28
M_DATA_B29	AL3	SB_DQ_29
M_DATA_B30	AR12	SB_DQ_30
M_DATA_B31	AP12	SB_DQ_31
M_DATA_B32	AR28	SB_DQ_32
M_DATA_B33	AR29	SB_DQ_33
M_DATA_B34	AL28	SB_DQ_34
M_DATA_B35	AL29	SB_DQ_35
M_DATA_B36	AP28	SB_DQ_36
M_DATA_B37	AP29	SB_DQ_37
M_DATA_B38	AM28	SB_DQ_38
M_DATA_B39	AM29	SB_DQ_39
M_DATA_B40	AP32	SB_DQ_40
M_DATA_B41	AP31	SB_DQ_41
M_DATA_B42	AP35	SB_DQ_42
M_DATA_B43	AP34	SB_DQ_43
M_DATA_B44	AR32	SB_DQ_44
M_DATA_B45	AR31	SB_DQ_45
M_DATA_B46	AR35	SB_DQ_46
M_DATA_B47	AR34	SB_DQ_47
M_DATA_B48	AM32	SB_DQ_48
M_DATA_B52	AM31	SB_DQ_49
M_DATA_B55	AL35	SB_DQ_50
M_DATA_B51	AL32	SB_DQ_51
M_DATA_B54	AM34	SB_DQ_52
M_DATA_B49	AL31	SB_DQ_53
M_DATA_B53	AM35	SB_DQ_54
M_DATA_B50	AL34	SB_DQ_55
M_DATA_B59	AH35	SB_DQ_56
M_DATA_B57	AH34	SB_DQ_57
M_DATA_B58	AE34	SB_DQ_58
M_DATA_B59	AE35	SB_DQ_59
M_DATA_B60	AJ35	SB_DQ_60
M_DATA_B61	AJ34	SB_DQ_61
M_DATA_B62	AF33	SB_DQ_62
M_DATA_B63	AF35	SB_DQ_63

M_DQS_B_P0	AH7	SB_DQS_0
M_DQS_B_P1	AM8	SB_DQS_1
M_DQS_B_P2	AR8	SB_DQS_2
M_DQS_B_P3	AN13	SB_DQS_3
M_DQS_B_P4	AN29	SB_DQS_4
M_DQS_B_P5	AP33	SB_DQS_5
M_DQS_B_P6	AL33	SB_DQS_6
M_DQS_B_P7	AG35	SB_DQS_7

M_DQS_B_N0	AH6	SB_DQS#_0
M_DQS_B_N1	AL8	SB_DQS#_1
M_DQS_B_N2	AP8	SB_DQS#_2
M_DQS_B_N3	AN12	SB_DQS#_3
M_DQS_B_N4	AN28	SB_DQS#_4
M_DQS_B_N5	AR33	SB_DQS#_5
M_DQS_B_N6	AM33	SB_DQS#_6
M_DQS_B_N7	AG34	SB_DQS#_7

CPU10

M_DATA_B0	AG7	SB_DQ_0
M_DATA_B1	AG8	SB_DQ_1
M_DATA_B2	AJ9	SB_DQ_2
M_DATA_B3	AJ8	SB_DQ_3
M_DATA_B4	AG5	SB_DQ_4
M_DATA_B5	AG6	SB_DQ_5
M_DATA_B6	AJ6	SB_DQ_6
M_DATA_B7	AJ7	SB_DQ_7
M_DATA_B13	AL7	SB_DQ_8
M_DATA_B9	AM7	SB_DQ_9
M_DATA_B11	AM10	SB_DQ_10
M_DATA_B15	AL10	SB_DQ_11
M_DATA_B12	AL6	SB_DQ_12
M_DATA_B8	AM6	SB_DQ_13
M_DATA_B14	AL9	SB_DQ_14
M_DATA_B10	AM9	SB_DQ_15
M_DATA_B16	AP7	SB_DQ_16
M_DATA_B17	AP7	SB_DQ_17
M_DATA_B18	AP10	SB_DQ_18
M_DATA_B19	AR10	SB_DQ_19
M_DATA_B20	AP6	SB_DQ_20
M_DATA_B21	AR6	SB_DQ_21
M_DATA_B22	AP9	SB_DQ_22
M_DATA_B23	AP9	SB_DQ_23
M_DATA_B24	AM12	SB_DQ_24
M_DATA_B25	AM13	SB_DQ_25
M_DATA_B26	AR13	SB_DQ_26
M_DATA_B27	AP13	SB_DQ_27
M_DATA_B28	AL12	SB_DQ_28
M_DATA_B29	AL3	SB_DQ_29
M_DATA_B30	AR12	SB_DQ_30
M_DATA_B31	AP12	SB_DQ_31
M_DATA_B32	AR28	SB_DQ_32
M_DATA_B33	AR29	SB_DQ_33
M_DATA_B34	AL28	SB_DQ_34
M_DATA_B35	AL29	SB_DQ_35
M_DATA_B36	AP28	SB_DQ_36
M_DATA_B37	AP29	SB_DQ_37
M_DATA_B38	AM28	SB_DQ_38
M_DATA_B39	AM29	SB_DQ_39
M_DATA_B40	AP32	SB_DQ_40
M_DATA_B41	AP31	SB_DQ_41
M_DATA_B42	AP35	SB_DQ_42
M_DATA_B43	AP34	SB_DQ_43
M_DATA_B44	AR32	SB_DQ_44
M_DATA_B45	AR31	SB_DQ_45
M_DATA_B46	AR35	SB_DQ_46
M_DATA_B47	AR34	SB_DQ_47
M_DATA_B48	AM32	SB_DQ_48
M_DATA_B52	AM31	SB_DQ_49
M_DATA_B55	AL35	SB_DQ_50
M_DATA_B51	AL32	SB_DQ_51
M_DATA_B54	AM34	SB_DQ_52
M_DATA_B49	AL31	SB_DQ_53
M_DATA_B53	AM35	SB_DQ_54
M_DATA_B50	AL34	SB_DQ_55
M_DATA_B59	AH35	SB_DQ_56
M_DATA_B57	AH34	SB_DQ_57
M_DATA_B58	AE34	SB_DQ_58
M_DATA_B59	AE35	SB_DQ_59
M_DATA_B60	AJ35	SB_DQ_60
M_DATA_B61	AJ34	SB_DQ_61
M_DATA_B62	AF33	SB_DQ_62
M_DATA_B63	AF35	SB_DQ_63

M_DQS_B_P0	AH7	SB_DQS_0
M_DQS_B_P1	AM8	SB_DQS_1
M_DQS_B_P2	AR8	SB_DQS_2
M_DQS_B_P3	AN13	SB_DQS_3
M_DQS_B_P4	AN29	SB_DQS_4
M_DQS_B_P5	AP33	SB_DQS_5
M_DQS_B_P6	AL33	SB_DQS_6
M_DQS_B_P7	AG35	SB_DQS_7

M_DQS_B_N0	AH6	SB_DQS#_0
M_DQS_B_N1	AL8	SB_DQS#_1
M_DQS_B_N2	AP8	SB_DQS#_2
M_DQS_B_N3	AN12	SB_DQS#_3
M_DQS_B_N4	AN28	SB_DQS#_4
M_DQS_B_N5	AR33	SB_DQS#_5
M_DQS_B_N6	AM33	SB_DQS#_6
M_DQS_B_N7	AG34	SB_DQS#_7

SKT_H2_CRB

DDR3 CH.B

BALLMAP_REV=1.4

SA_CK[2]
SA_CK[1]
SA_ODT[2]

SB_BS_0
SB_BS_1
SB_BS_2

SB_CS#_0
SB_CS#_1
SB_CS#_2
SB_CS#_3

SB_CKE_0
SB_CKE_1
SB_CKE_2
SB_CKE_3

SB_ODT_0
SB_ODT_1
SB_ODT_2
SB_ODT_3

SB_CK_0
SB_CK#_0
SB_CK_1
SB_CK#_1
SB_CK_2
SB_CK#_2
SB_CK_3
SB_CK#_3

SB_DQS_8
SB_DQS#_8

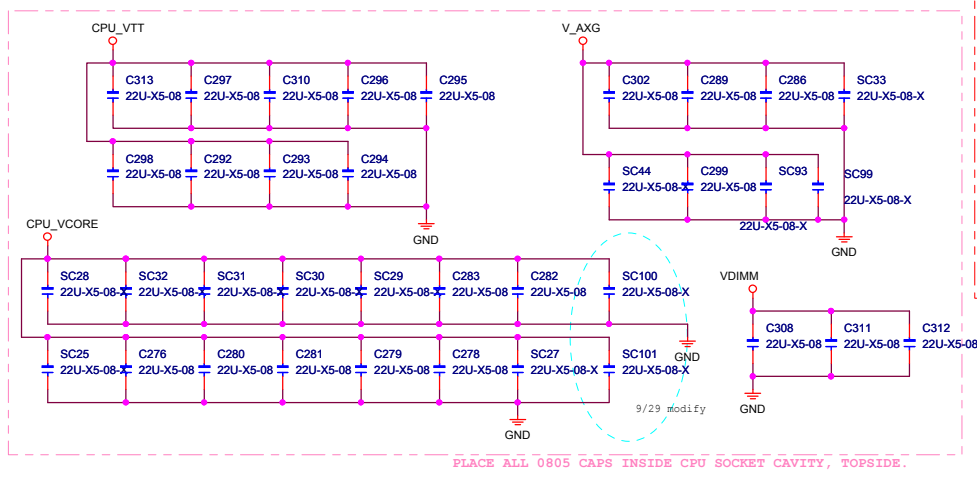
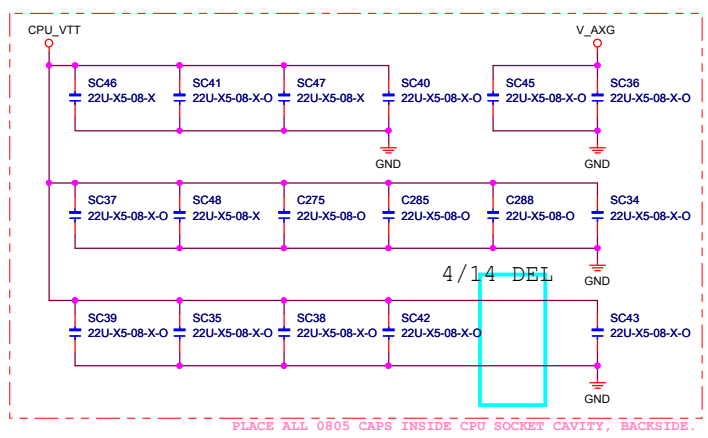
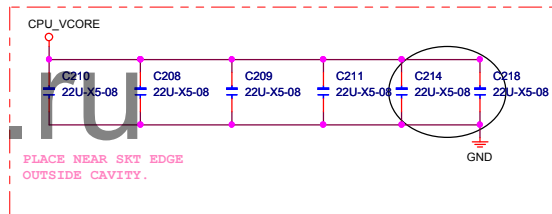
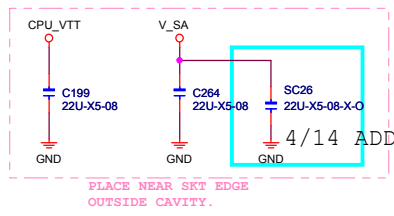
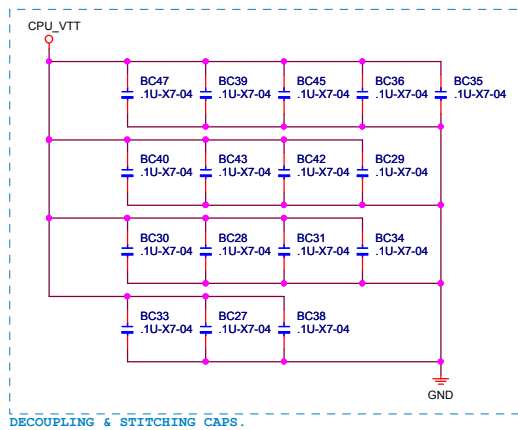
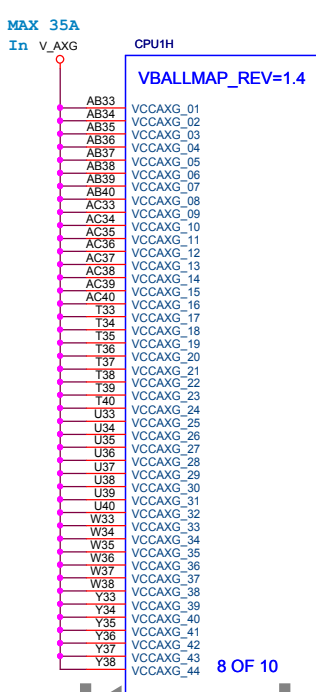
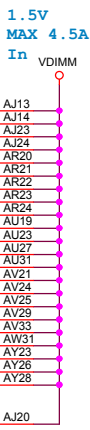
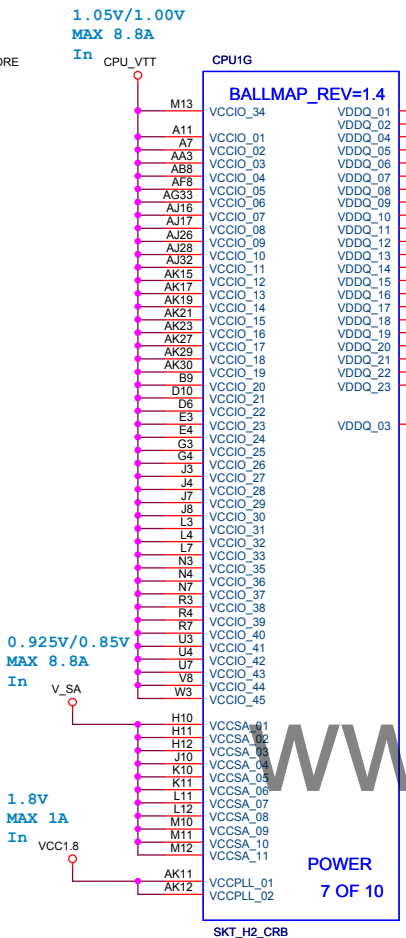
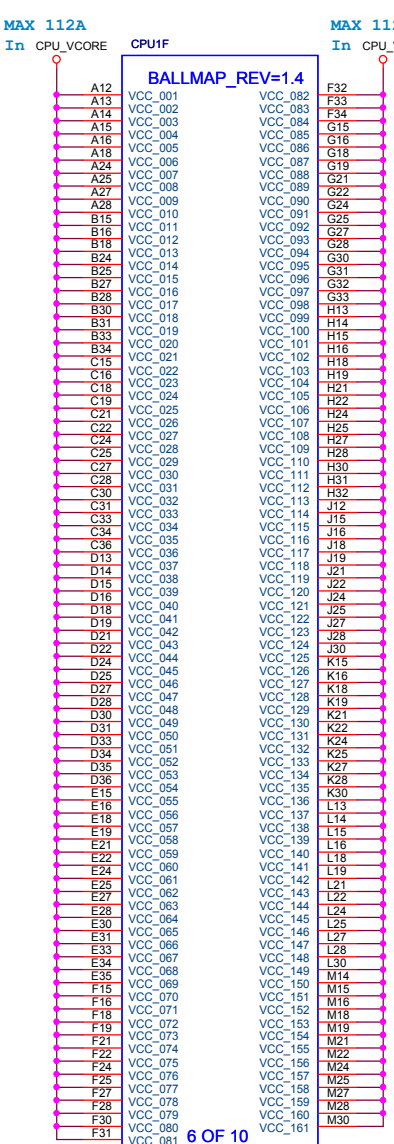
SB_ECC_CB_0
SB_ECC_CB_1
SB_ECC_CB_2
SB_ECC_CB_3
SB_ECC_CB_4
SB_ECC_CB_5
SB_ECC_CB_6
SB_ECC_CB_7

DDR_1

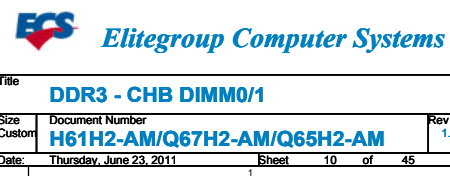
4 OF 10

AK24	M_MA_B0
AM20	M_MA_B1
AM19	M_MA_B2
AK18	M_MA_B3
AP19	M_MA_B4
AP18	M_MA_B5
AM18	M_MA_B6
AL18	M_MA_B7
AN18	M_MA_B8
AY17	M_MA_B9
AN23	M_MA_B10
AU17	M_MA_B11
AT18	M_MA_B12
AR26	M_MA_B13
AY16	M_MA_B14
AV16	M_MA_B15

AR25 M_WE_B_L
AK



CPU11				CPU1J			
BALLMAP_REV=1.4				BALLMAP_REV=1.4			
A17	VSS_001	VSS_091	AM27	AV11	VSS_181	VSS_271	G8
A23	VSS_002	VSS_092	AM3	AV14	VSS_182	VSS_272	H1
A26	VSS_003	VSS_093	AM30	AV17	VSS_183	VSS_273	H17
A29	VSS_004	VSS_094	AM36	AV3	VSS_184	VSS_274	H2
A35	VSS_005	VSS_095	AM37	AV35	VSS_185	VSS_275	H20
AA33	VSS_005	VSS_095	AM38	AV38	VSS_185	VSS_275	H23
AA34	VSS_006	VSS_096	AM39	AV6	VSS_186	VSS_276	H26
AA35	VSS_007	VSS_097	AM4	AW10	VSS_187	VSS_277	H29
AA36	VSS_008	VSS_098	AM40	AW11	VSS_188	VSS_278	H33
AA37	VSS_009	VSS_099	AM5	AW14	VSS_189	VSS_279	H35
AA38	VSS_010	VSS_100	AM10	AW16	VSS_190	VSS_280	H37
AA6	VSS_011	VSS_101	AN11	AW36	VSS_191	VSS_281	H39
AB5	VSS_012	VSS_102	AN12	AW6	VSS_192	VSS_282	H5
AC1	VSS_013	VSS_103	AN14	AY11	VSS_193	VSS_283	H6
AC6	VSS_014	VSS_104	AN17	AY14	VSS_194	VSS_284	H9
AD33	VSS_015	VSS_105	AN19	AY18	VSS_195	VSS_285	J11
AD33	VSS_016	VSS_106	AN22	AY35	VSS_196	VSS_286	J17
AD38	VSS_017	VSS_107	AN27	AY6	VSS_197	VSS_287	J20
AD39	VSS_018	VSS_108	AN30	AY4	VSS_198	VSS_288	J23
AD40	VSS_019	VSS_109	AN31	AY8	VSS_199	VSS_289	J26
AD5	VSS_021	VSS_110	AN32	B10	VSS_200	VSS_290	J29
AD8	VSS_022	VSS_111	AN33	B13	VSS_201	VSS_291	J32
AE3	VSS_023	VSS_112	AN34	B14	VSS_202	VSS_292	K1
AE33	VSS_023	VSS_113	AN35	B17	VSS_203	VSS_293	K12
AE36	VSS_024	VSS_114	AN36	B23	VSS_204	VSS_294	K13
AF1	VSS_025	VSS_115	AN5	B26	VSS_205	VSS_295	K14
AF34	VSS_026	VSS_116	AN6	B29	VSS_206	VSS_296	K17
AF36	VSS_027	VSS_117	AN7	B32	VSS_207	VSS_297	K2
AF37	VSS_028	VSS_118	AN8	B35	VSS_208	VSS_298	K20
AF40	VSS_029	VSS_119	AN9	B38	VSS_209	VSS_299	K23
AF5	VSS_030	VSS_120	AP1	B6	VSS_210	VSS_300	K26
AF6	VSS_031	VSS_121	AP11	C11	VSS_211	VSS_301	K29
AF7	VSS_032	VSS_122	AP17	C12	VSS_212	VSS_302	K33
AG36	VSS_033	VSS_123	AP17	C17	VSS_213	VSS_303	K35
AH2	VSS_034	VSS_124	AP22	C20	VSS_214	VSS_304	K37
AH3	VSS_035	VSS_125	AP25	C23	VSS_215	VSS_305	K39
AH33	VSS_036	VSS_126	AP27	C26	VSS_216	VSS_306	K5
AH36	VSS_037	VSS_127	AP30	C29	VSS_217	VSS_307	K6
AH37	VSS_038	VSS_128	AP36	C32	VSS_218	VSS_308	L10
AH38	VSS_039	VSS_129	AP37	C35	VSS_219	VSS_309	L17
AH39	VSS_040	VSS_130	AP4	C7	VSS_220	VSS_310	L20
AH40	VSS_041	VSS_131	AP40	C8	VSS_221	VSS_311	L23
AH5	VSS_042	VSS_132	AP5	D17	VSS_222	VSS_312	L26
AH8	VSS_043	VSS_133	AR11	D2	VSS_223	VSS_313	L29
AJ12	VSS_044	VSS_134	AR14	D20	VSS_224	VSS_314	L8
AJ15	VSS_045	VSS_135	AR17	D23	VSS_225	VSS_315	M1
AJ18	VSS_046	VSS_136	AR18	D26	VSS_226	VSS_316	M17
AJ21	VSS_047	VSS_137	AR19	D29	VSS_227	VSS_317	M2
AJ25	VSS_048	VSS_138	AR27	D32	VSS_228	VSS_318	M20
AJ27	VSS_049	VSS_139	AR30	D32	VSS_229	VSS_319	M23
AJ36	VSS_050	VSS_140	AR36	D39	VSS_230	VSS_320	M29
AJ5	VSS_051	VSS_141	AR5	D4	VSS_231	VSS_321	M29
AK1	VSS_052	VSS_142	AT1	D5	VSS_232	VSS_322	M33
AK10	VSS_053	VSS_143	AT10	D9	VSS_233	VSS_323	M35
AK13	VSS_054	VSS_144	AT12	D9	VSS_234	VSS_324	M35
AK13	VSS_055	VSS_145	AT12	E11	VSS_235	VSS_325	M37
AK14	VSS_056	VSS_146	AT13	E12	VSS_236	VSS_326	M39
AK16	VSS_056	VSS_146	AT15	E17	VSS_236	VSS_326	M5
AK22	VSS_057	VSS_147	AT16	E20	VSS_237	VSS_327	M6
AK28	VSS_058	VSS_148	AT17	E23	VSS_238	VSS_328	M9
AK31	VSS_059	VSS_149	AT2	E26	VSS_239	VSS_329	N8
AK32	VSS_060	VSS_150	AT25	E29	VSS_240	VSS_330	P1
AK33	VSS_061	VSS_151	AT27	E32	VSS_241	VSS_331	P2
AK34	VSS_062	VSS_152	AT28	E36	VSS_242	VSS_332	P36
AK35	VSS_063	VSS_153	AT29	E7	VSS_243	VSS_333	P38
AK36	VSS_064	VSS_154	AT3	E8	VSS_244	VSS_334	P40
AK36	VSS_065	VSS_155	AT3	E7	VSS_245	VSS_335	P40
AK37	VSS_066	VSS_156	AT30	F1	VSS_246	VSS_336	P5
AK4	VSS_067	VSS_157	AT31	F10	VSS_247	VSS_337	P6
AK40	VSS_068	VSS_158	AT32	F13	VSS_247	VSS_337	R33
AK5	VSS_068	VSS_158	AT33	F14	VSS_248	VSS_338	R35
AK6	VSS_069	VSS_159	AT34	F17	VSS_249	VSS_339	R37
AK7	VSS_070	VSS_160	AT35	F2	VSS_250	VSS_340	R39
AK8	VSS_071	VSS_161	AT36	F23	VSS_251	VSS_341	R39
AK9	VSS_072	VSS_162	AT37	F39	VSS_252	VSS_342	T1
AL11	VSS_073	VSS_163	AT38	F26	VSS_253	VSS_343	T5
AL14	VSS_074	VSS_164	AT39	F29	VSS_254	VSS_344	T6
AL17	VSS_075	VSS_165	AT4	F35	VSS_255	VSS_345	U8
AL19	VSS_076	VSS_166	AT40	F37	VSS_256	VSS_346	U1
AL24	VSS_077	VSS_167	AT5	F39	VSS_257	VSS_347	V2
AL27	VSS_078	VSS_168	AT6	F5	VSS_258	VSS_348	V33
AL30	VSS_079	VSS_169	AT7	F6	VSS_259	VSS_349	V34
AL36	VSS_080	VSS_170	AT8	F9	VSS_260	VSS_350	V35
AL5	VSS_081	VSS_171	AT9	G11	VSS_261	VSS_351	V36
AM1	VSS_082	VSS_172	AT19	G19	VSS_262	VSS_352	V37
AM11	VSS_083	VSS_173	AU1	G12	VSS_263	VSS_353	V37
AM11	VSS_084	VSS_174	AU15	G13	VSS_264	VSS_354	V38
AM17	VSS_085	VSS_175	AU26	G20	VSS_265	VSS_355	V39
AM17	VSS_085	VSS_175	AU34	G23	VSS_265	VSS_355	V40
AM2	VSS_086	VSS_176	AU4	G26	VSS_266	VSS_356	V5
AM2	VSS_087	VSS_177	AU6	G29	VSS_267	VSS_357	V6
AM21	VSS_088	VSS_178	AU8	G29	VSS_268	VSS_358	Y6
AM23	VSS_089	VSS_179	AU8	G34	VSS_269	VSS_359	Y6
AM25	VSS_090	VSS_180	AV10	G7	VSS_270	VSS_360	Y8
A4	VSS_NCTF_01			AY37	VSS_NCTF_03		
AV39	VSS_NCTF_02			B3	VSS_NCTF_04		
9 Of 10				10 of 10			



MOBILE ONLY, NOT FOR DESKTOP.
CRB CONNECT TO MINI PCIE.

STP16 1 PCH_CL_CLK1 BA50
STP15 1 PCH_CL_DATA1 BF50
STP17 1 PCH_CL_RST1 L BF49

PCH MEPWROK R BC48

ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0,
ALSO SUPPORT SATA2.0, SATA1.0.

ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0,
ALSO SUPPORT SATA2.0, SATA1.0.

FAN FUNCTION JUST FOR MOBILE

0408 del

GPIO17 BT17 TACH0_GPIO17
GPIO1 OBR BR19 TACH1_GPIO1
Over temp BA22 TACH2_GPIO6
GPIO7 BR16 TACH3_GPIO7
GPIO68 BU16 TACH4_GPIO68
GPIO69 BM18 TACH5_GPIO69
GPIO71 BN17 TACH6_GPIO70
GPIO71 BP15 TACH7_GPIO71

SCLOCK_GPIO22
SLOAD_GPIO38
SDATAOUT0_GPIO39
SDATAOUT1_GPIO48

PCH1C

CL_CLK1 BA50
CL_DATA1 BF50
CL_RST1# BF49

APWROK BN21
PWM0 BT21
PWM1 BM20
PWM2 BN19
PWM3

TACH0_GPIO17
TACH1_GPIO1
TACH2_GPIO6
TACH3_GPIO7
TACH4_GPIO68
TACH5_GPIO69
TACH6_GPIO70
TACH7_GPIO71

SST BC48

GPIO22 BA53
GPIO38 BE54
GPIO39 BF55
GPIO48 AW53

NC_1 AY20

IN OUT

AC56 SATA3P0_RX_N0
AB55 SATA3P0_RX_P0
AE46 SATA3P0_TX_N0
AE44 SATA3P0_TX_P0

AA53 SATA3P0_RX_N1
AA56 SATA3P0_RX_P1
AG49 SATA3P0_TX_N1
AG47 SATA3P0_TX_P1

AL50 SATA2P0_RX_N2
AL49 SATA2P0_RX_P2
AL56 SATA2P0_TX_N2
AL53 SATA2P0_TX_P2

AN46 SATA2P0_RX_N3
AN44 SATA2P0_RX_P3
AN56 SATA2P0_TX_N3
AM55 SATA2P0_TX_P3

AN49 SATA2P0_RX_N4
AN60 SATA2P0_RX_P4
AT50 SATA2P0_TX_N4
AT49 SATA2P0_TX_P4

AT48 SATA2P0_RX_N5
AT44 SATA2P0_RX_P5
AV50 SATA2P0_TX_N5
AV49 SATA2P0_TX_P5

AF55 CKG_SATA_N
AG56 CKG_SATA_P

BF57 SATALED_L
AJ55 SATALED_P
AJ53 SATA1RCOMP

BC54 GPIO21
AY52 GPIO19
BB55 GPIO36
BG53 GPIO37
AU56 GPIO16
BA56 GPIO49

SATA3COMP1
SATA3RCOMP

TP16
SATA3RBIAS
A20GATE
BN56 INT3_3V_L
B556 KB_RST_L
AV52 SER_IRQ
E56407 APD_P5 SP14 SHORT PAD
H48 PCSI
F55 PM_SYNC

PCH_1P05V

PCH_1P05V

GPIO19 12

R489 37.4-1-04

R490 49.9-1-04

R491 750-1-04

A20GATE 27

KB_RST_L 27

SER_IRQ 27

SP14 SHORT PAD

SP13

PM_SYNC 5

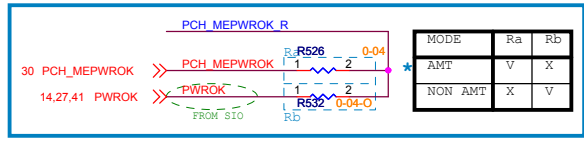
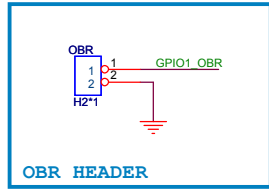
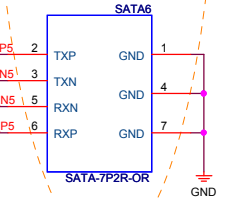
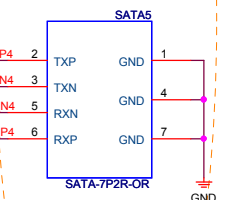
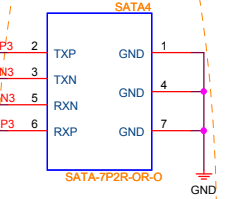
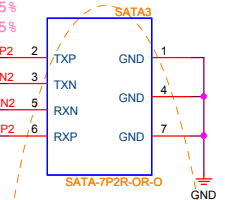
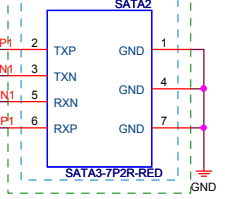
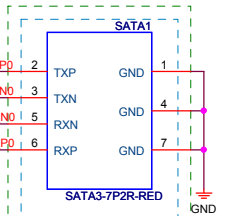
SATA1, SATA2 for Q67
SATA1 for Q65

SATA3, SATA4 for Q67, Q65

Layout Note:
SATA3.0 4.5/7.5/20 in 90 Ω ±17.5%
SATA2.0 4.5/7.5/15 in 90 Ω ±17.5%

Q67, Q65 need SATA3, SATA4,

0617 change footprint to sata7p-m-huanxun

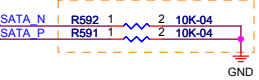
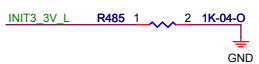
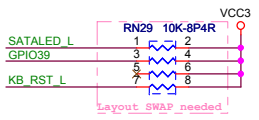
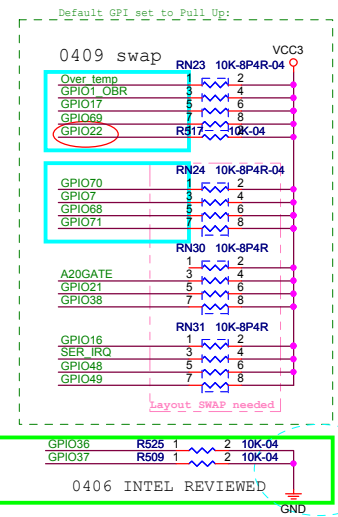


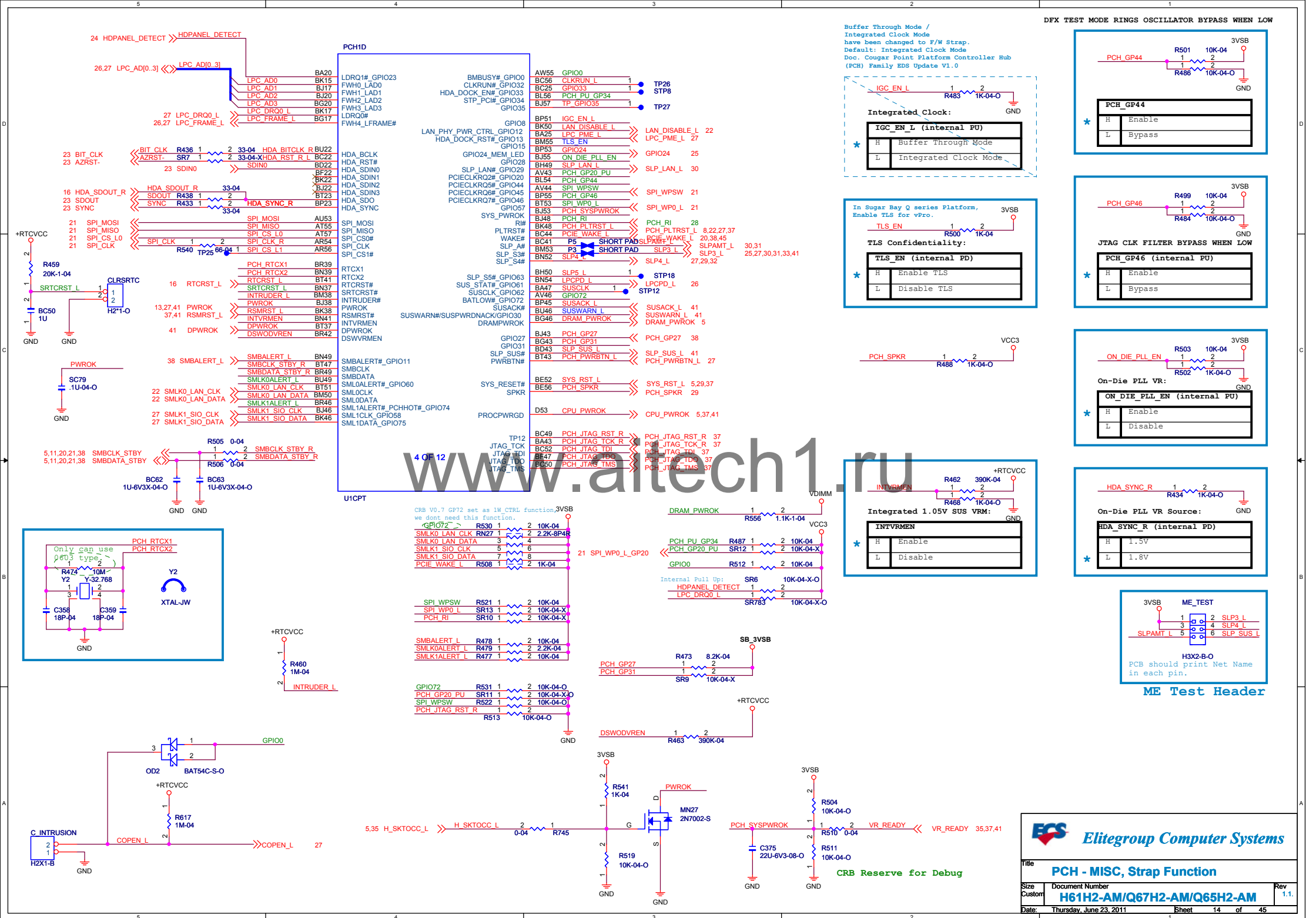
R532 for H61
R526 for Q67, Q65

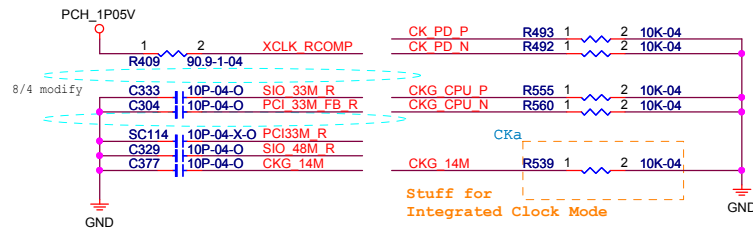
www.dleech1.ru

3 OF 12

U1CPT

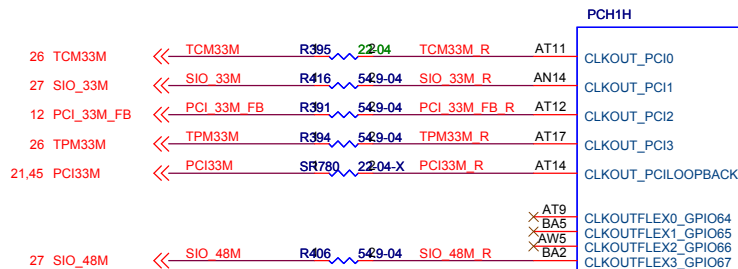




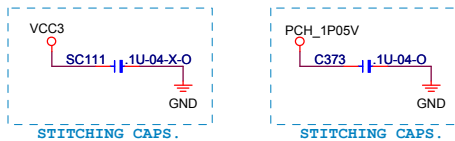
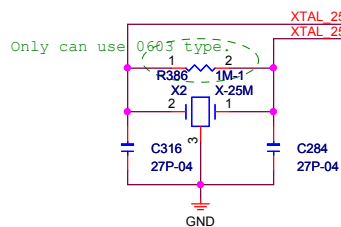


10'03'24

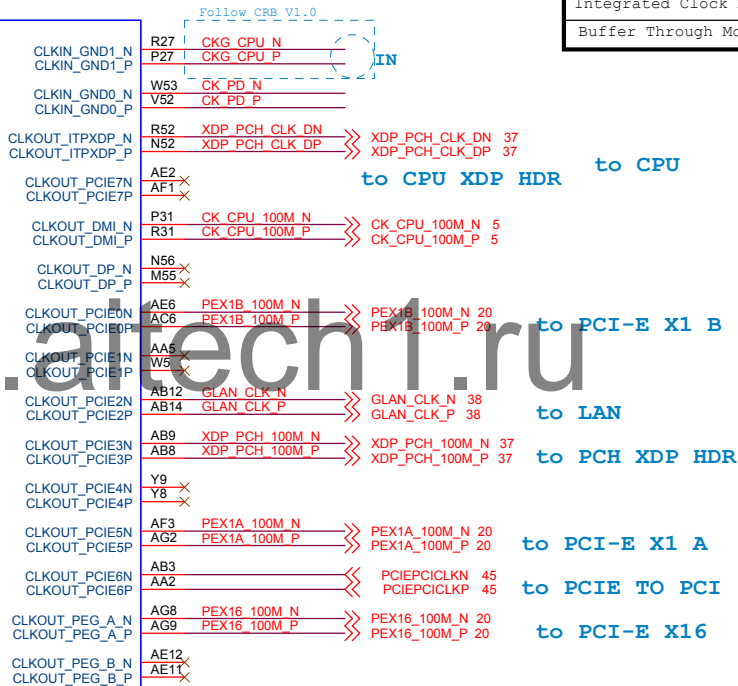
Clock Mode	CLK GEN. Seligo SLG421 Circuit.	CKa
Integrated Clock Mode	X	V
Buffer Through Mode	V	X



Layout Note:
PCI Clock Max 15000MILS



8 of 12

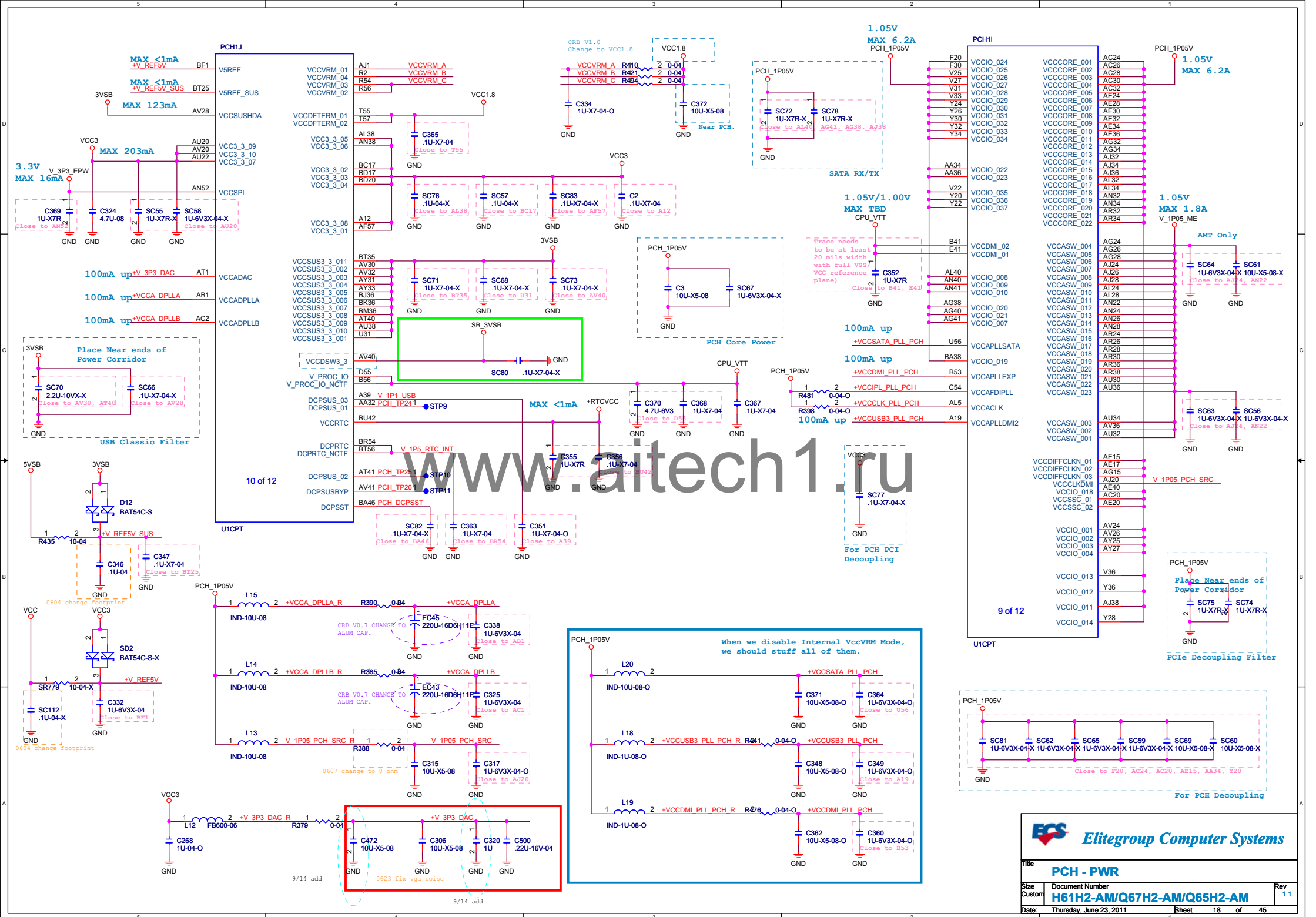


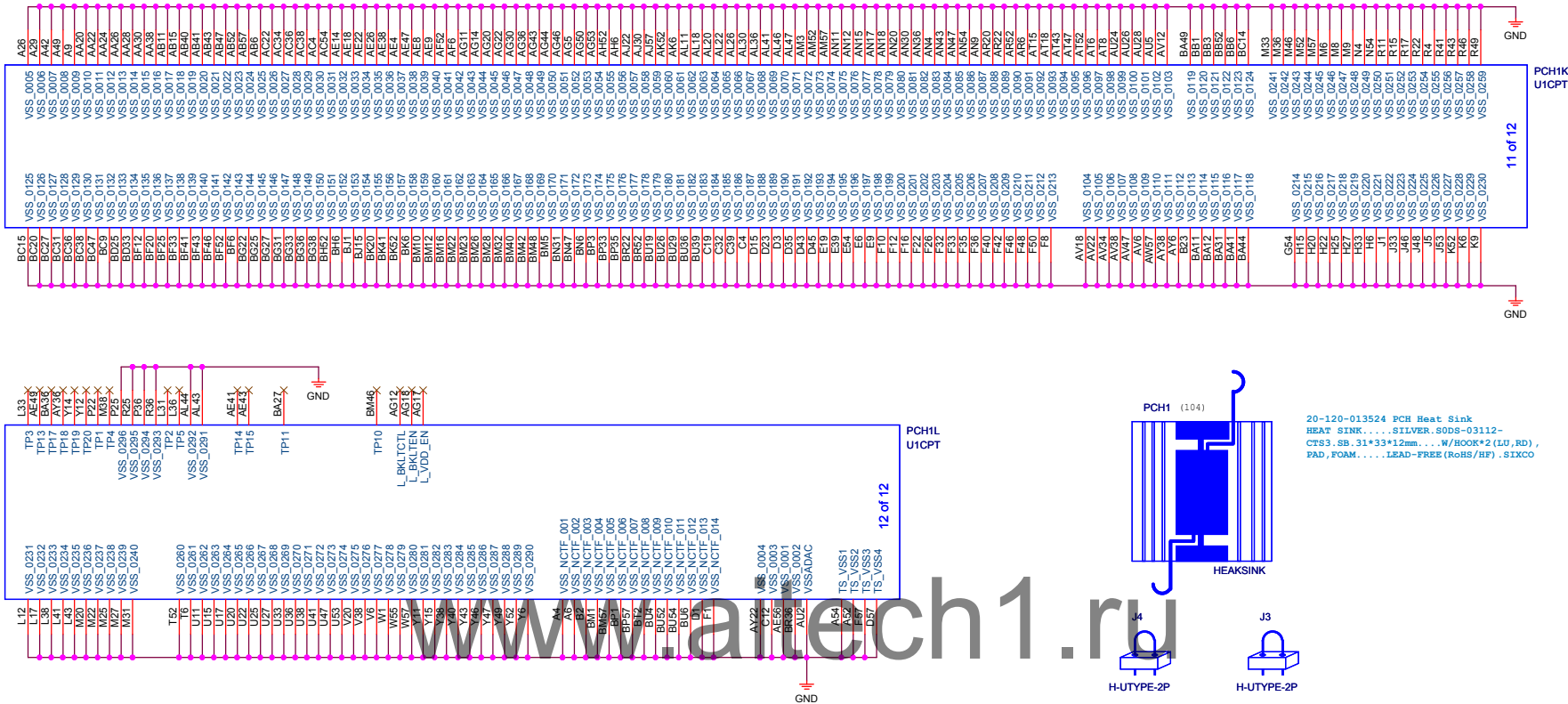
ECS Elitegroup Computer Systems

Title: **PCH - CLK IO, CKG - SLG421**

Size: **H61H2-AM/Q67H2-AM/Q65H2-AM** Rev: **1.1.**

Date: Thursday, June 23, 2011 Sheet: 15 of 45

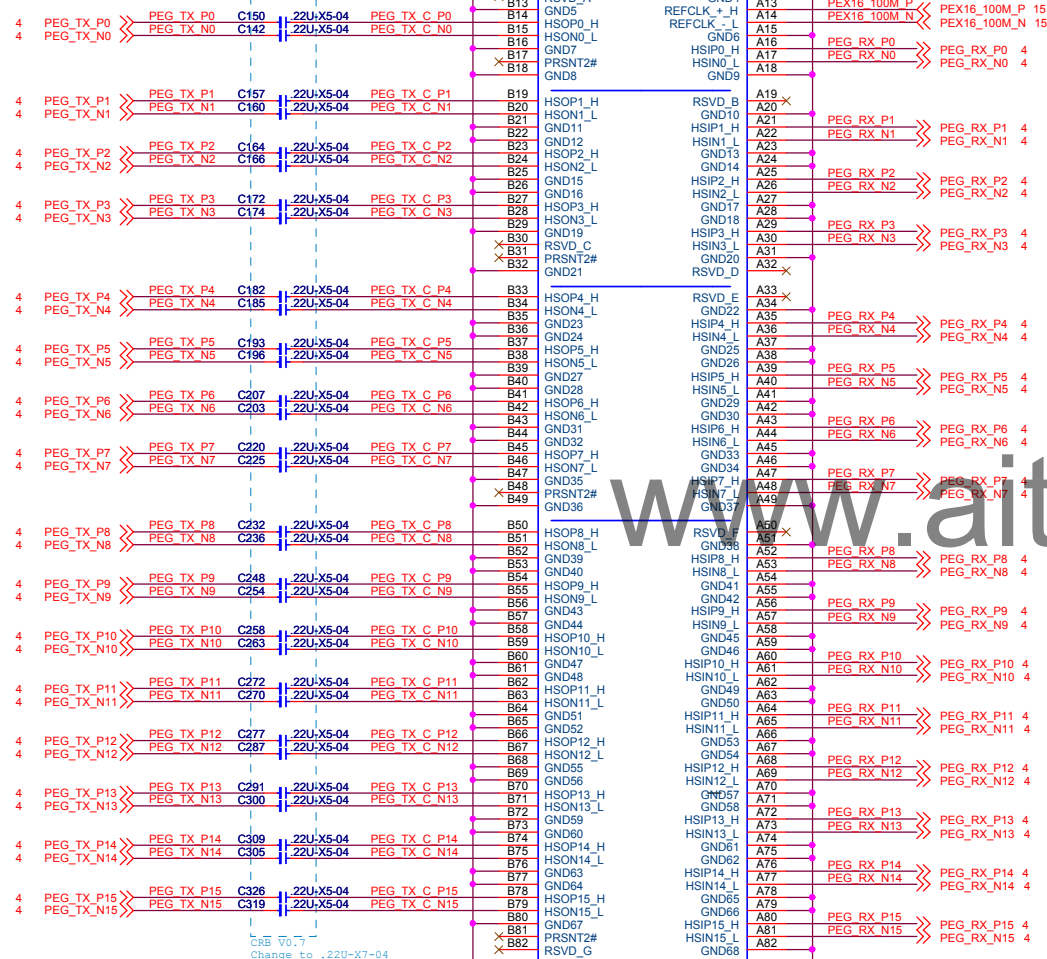




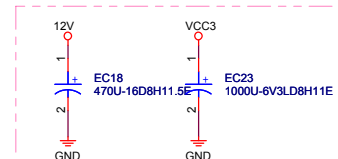
PCI-E X16 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A

5,11,14,21,38 SMBCLK_STBY
5,11,14,21,38 SMBDATA_STBY

14,38,45 PCIE_WAKE_L

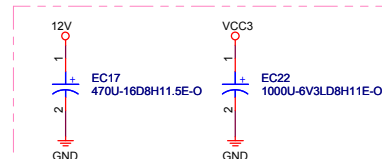


04-711-102073
E/C.1000uF.16V.20%...105C.RT D10*17mm....



Between PEX16 & PEX1A

04-711-102073
E/C.1000uF.16V.20%...105C.RT D10*17mm....

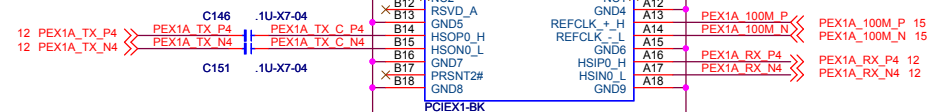


Between PEX1A & PEX1B

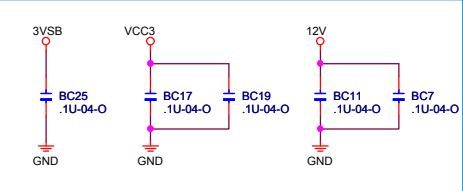
PCI-E X1 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/0.5A
+3VSB/0.375A

SMBCLK_STBY
SMBDATA_STBY

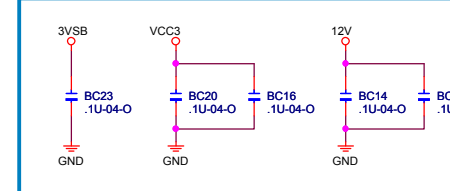
PCIE_WAKE_L



PCI-E X1 A



PCI-E X1 A Decoupling Cap.

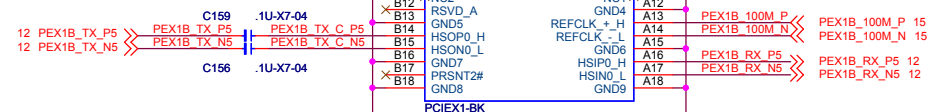


PCI-E X1 B Decoupling Cap.

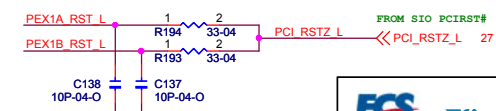
PCI-E X1 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/0.5A
+3VSB/0.375A

SMBCLK_STBY
SMBDATA_STBY

PCIE_WAKE_L

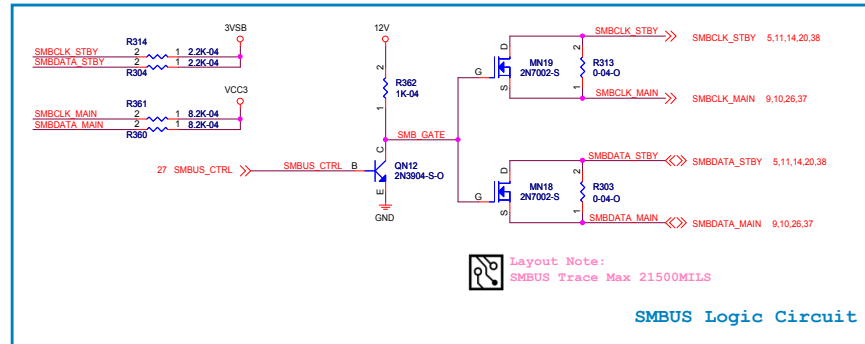
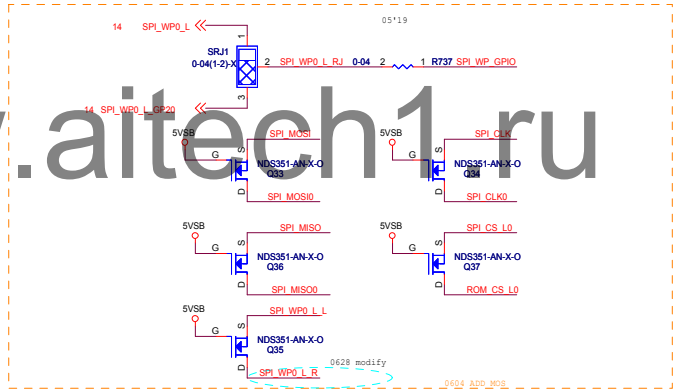
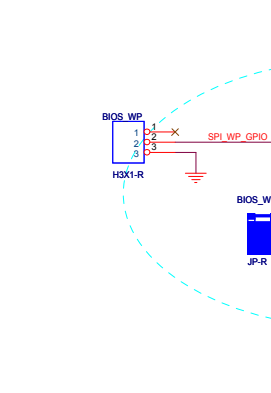
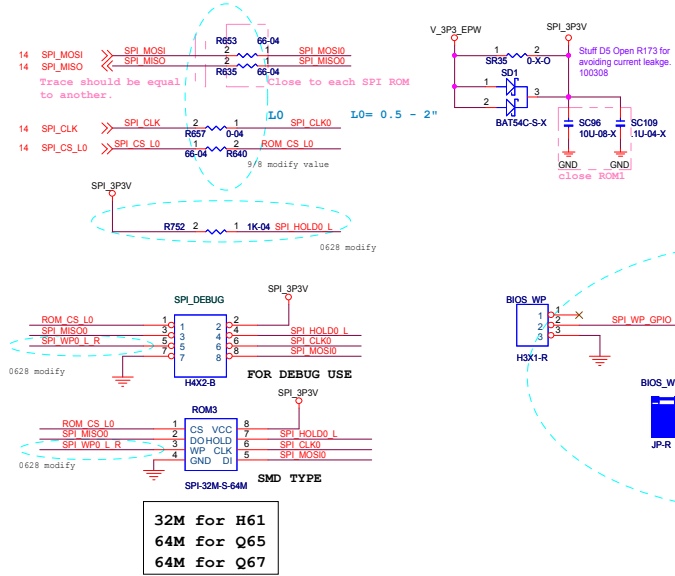
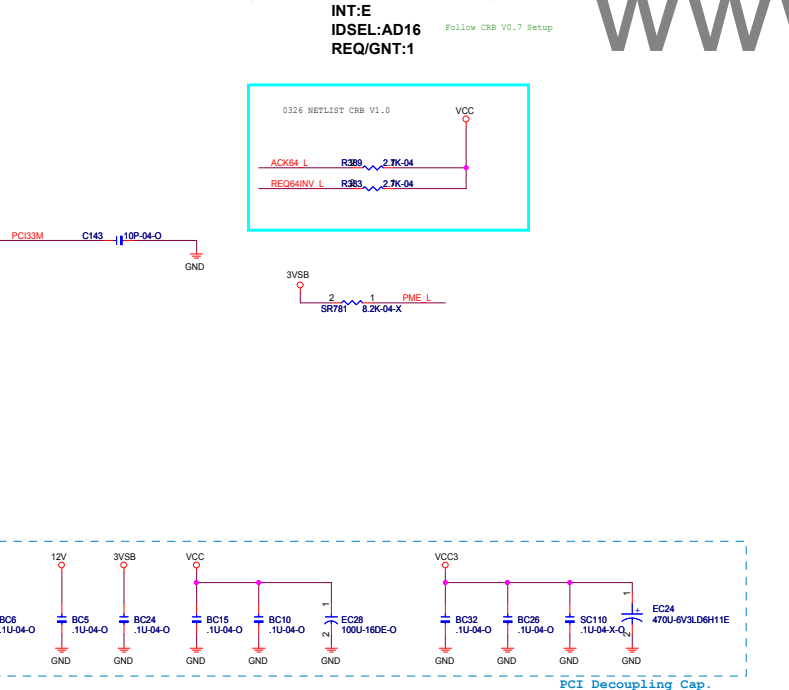


PCI-E X1 B

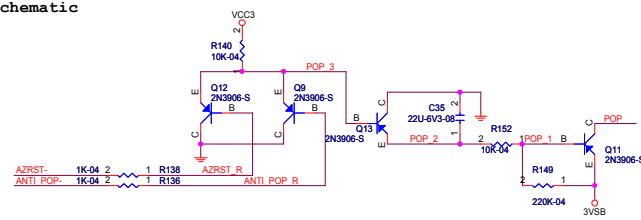


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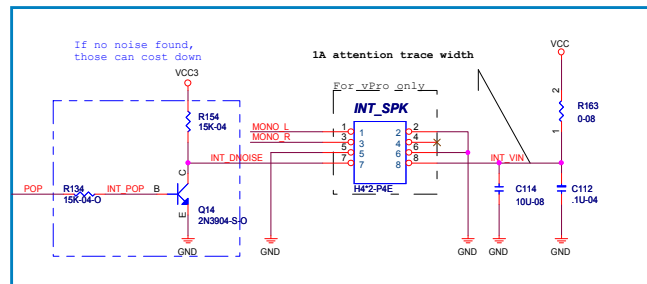
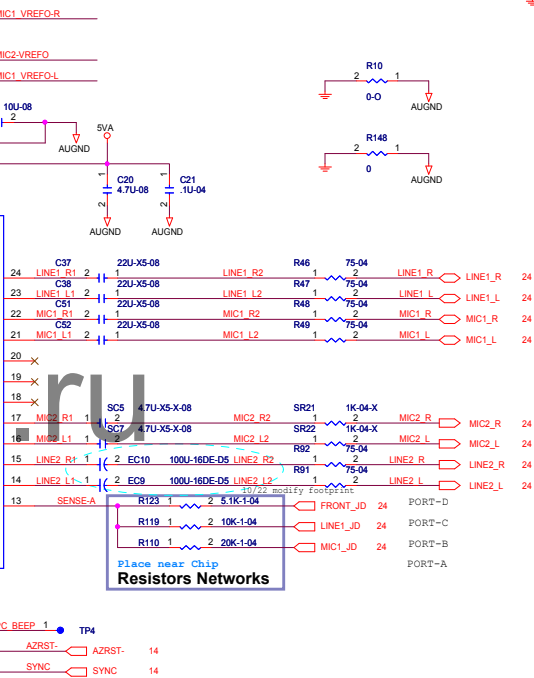
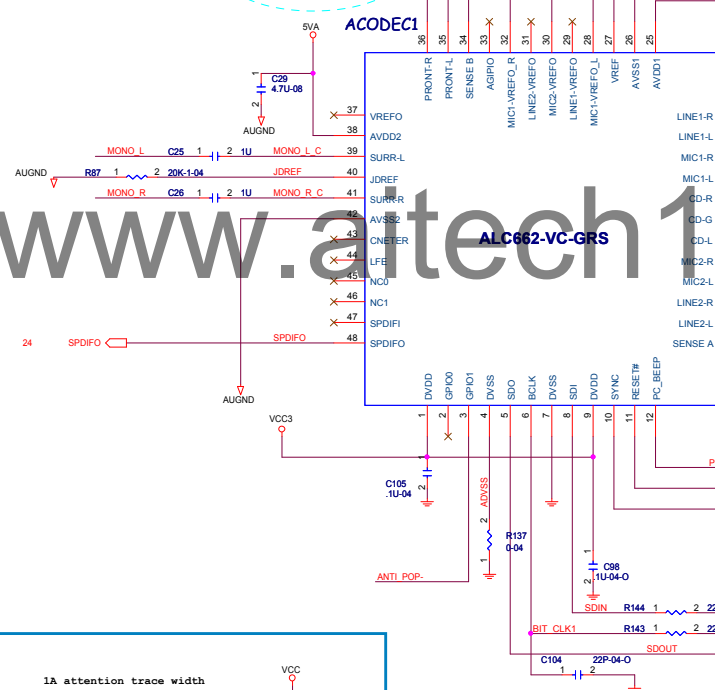
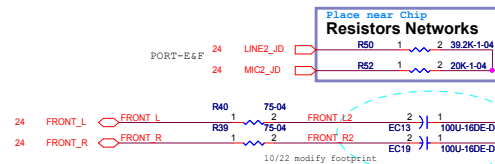
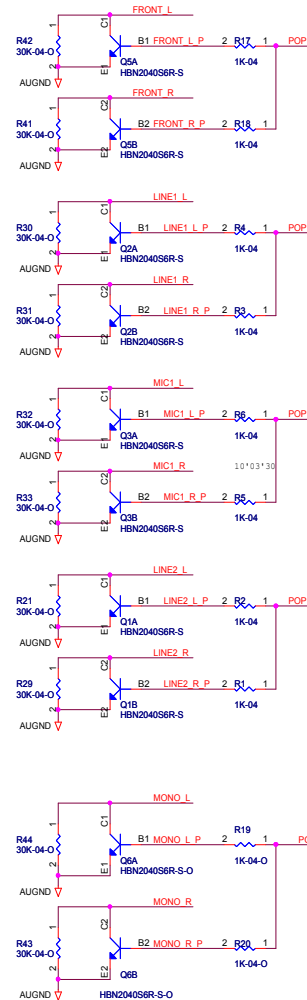
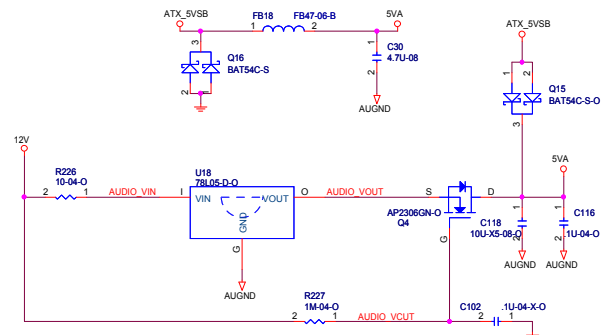
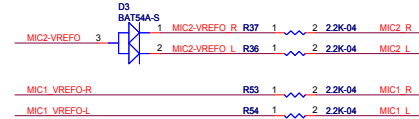
Slot - PCI-EX16/PCI-EX1		
Size	Document Number	Rev
Custom	H61H2-AM/Q67H2-AM/Q65H2-AM	1.1.
Date:	Thursday, June 23, 2011	Sheet 20 of 45

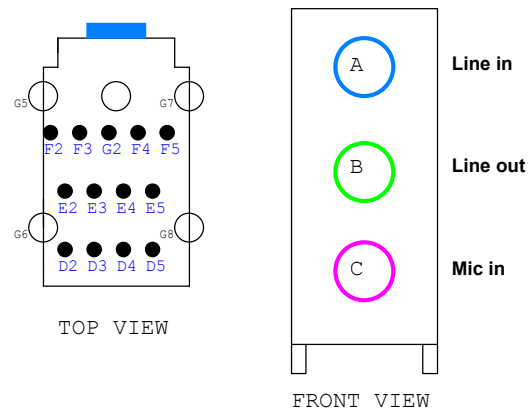
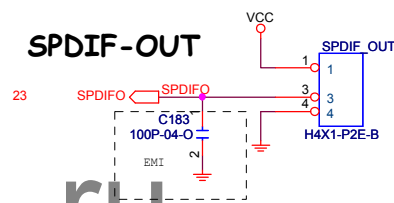
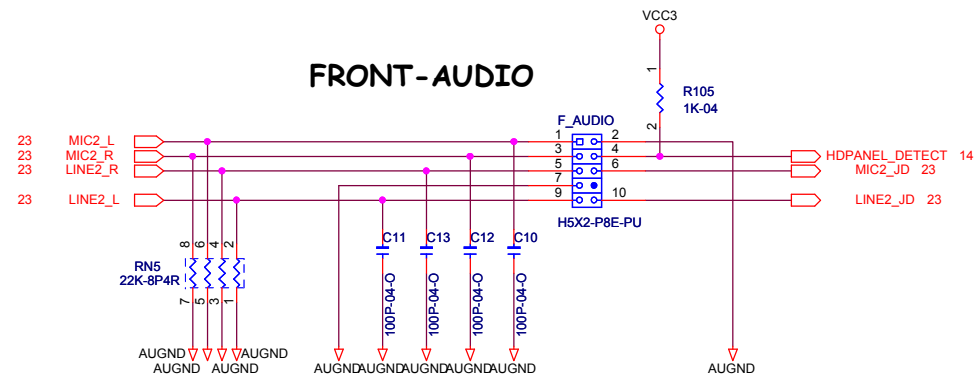
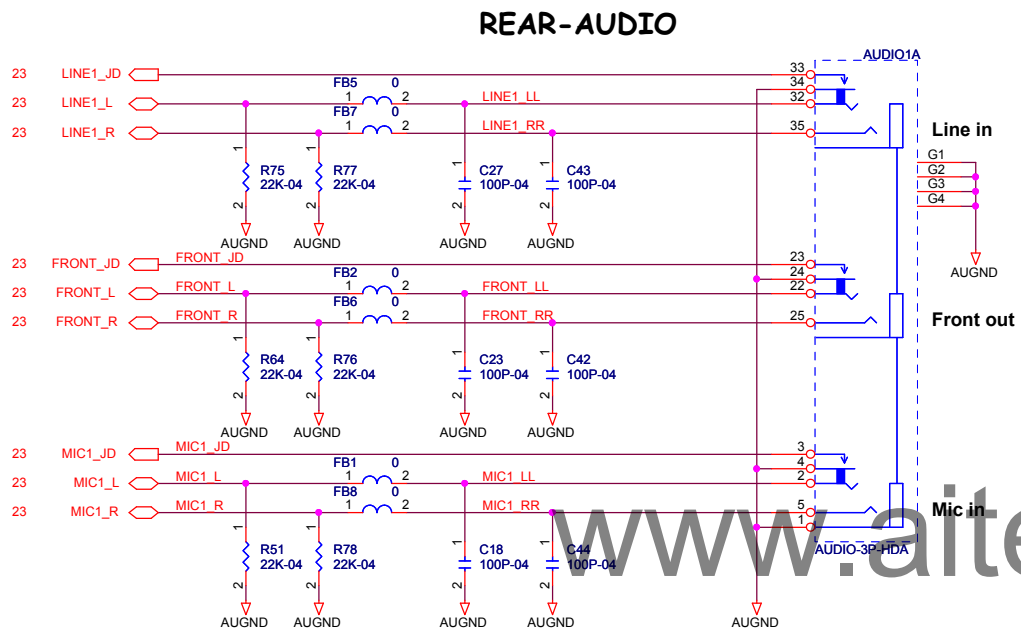


Depop schematic

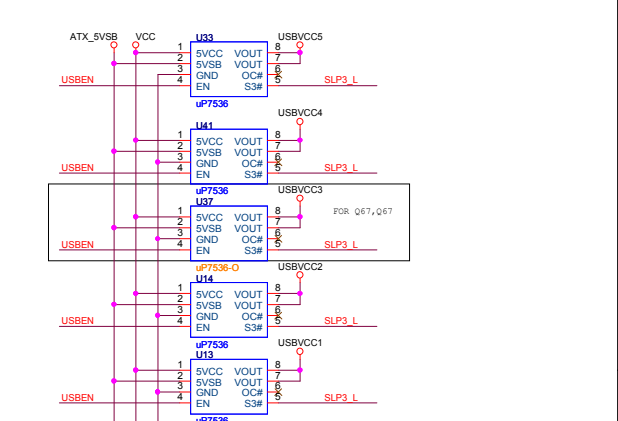
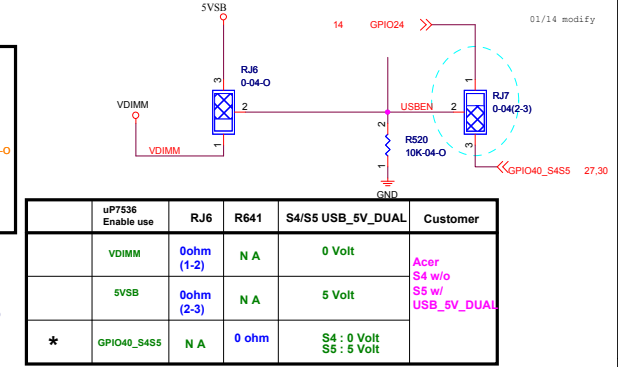
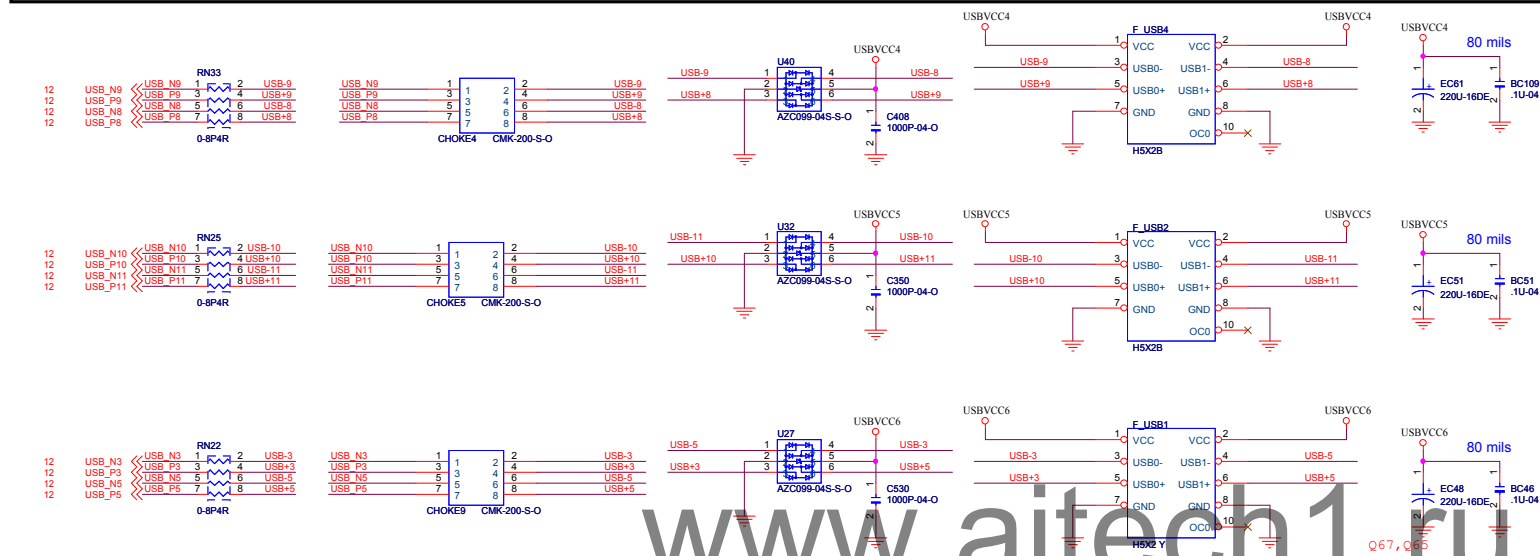
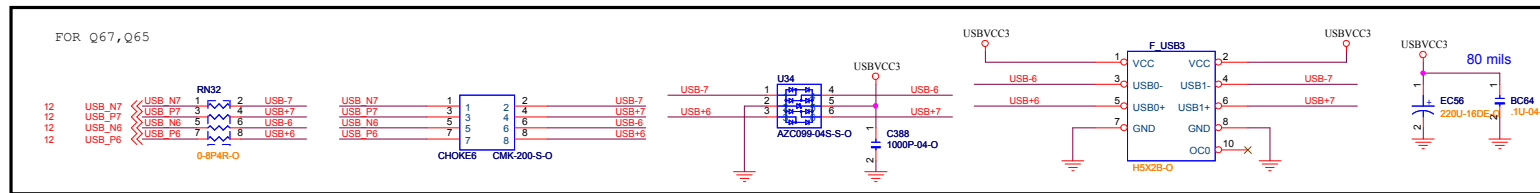


MIC Bias



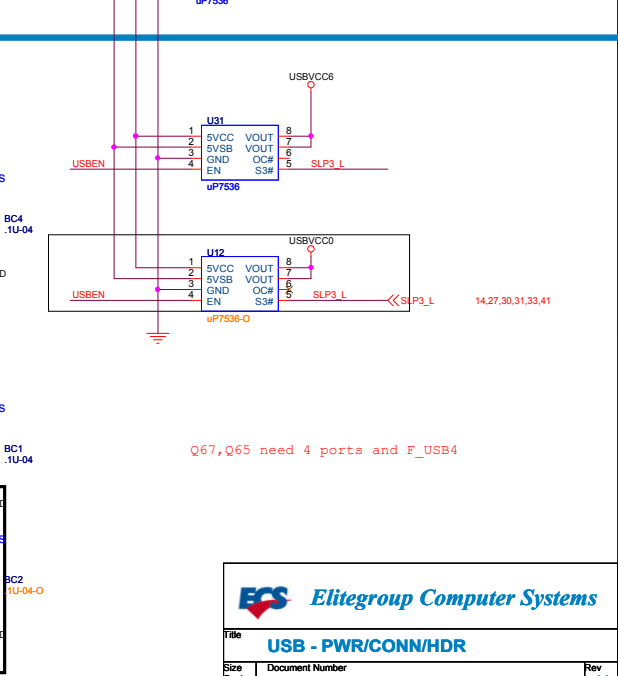
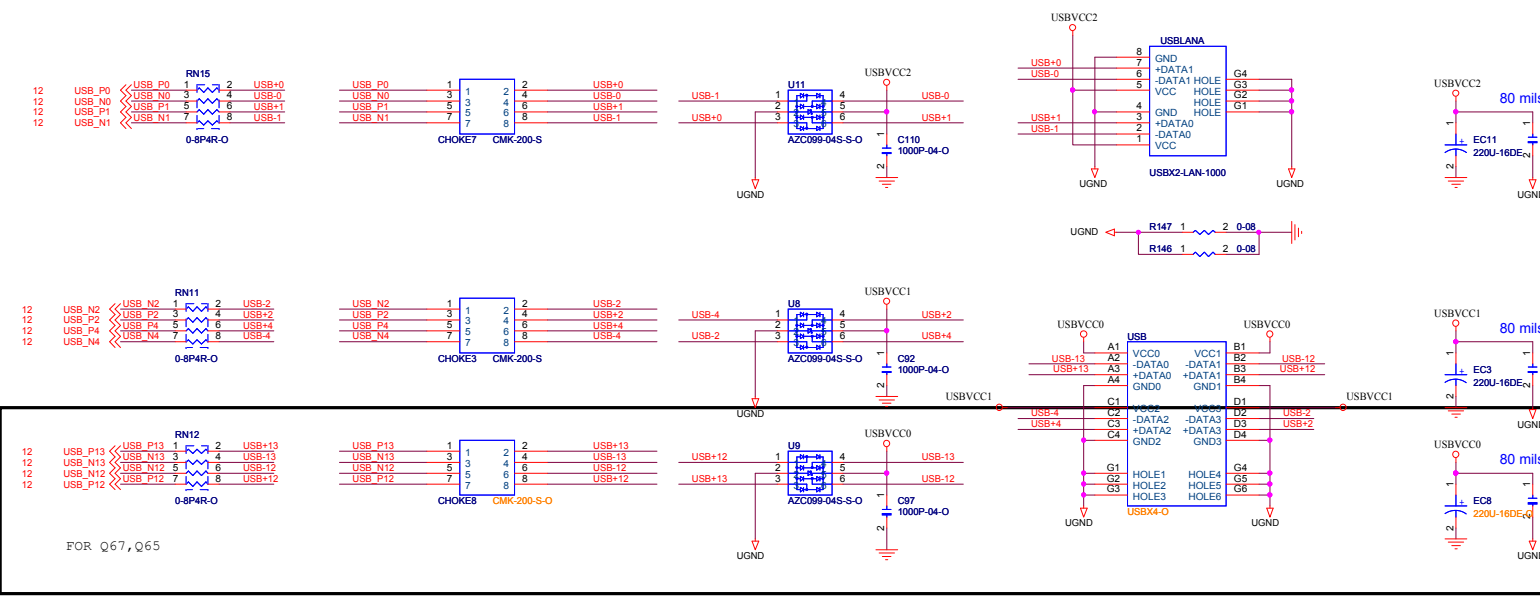


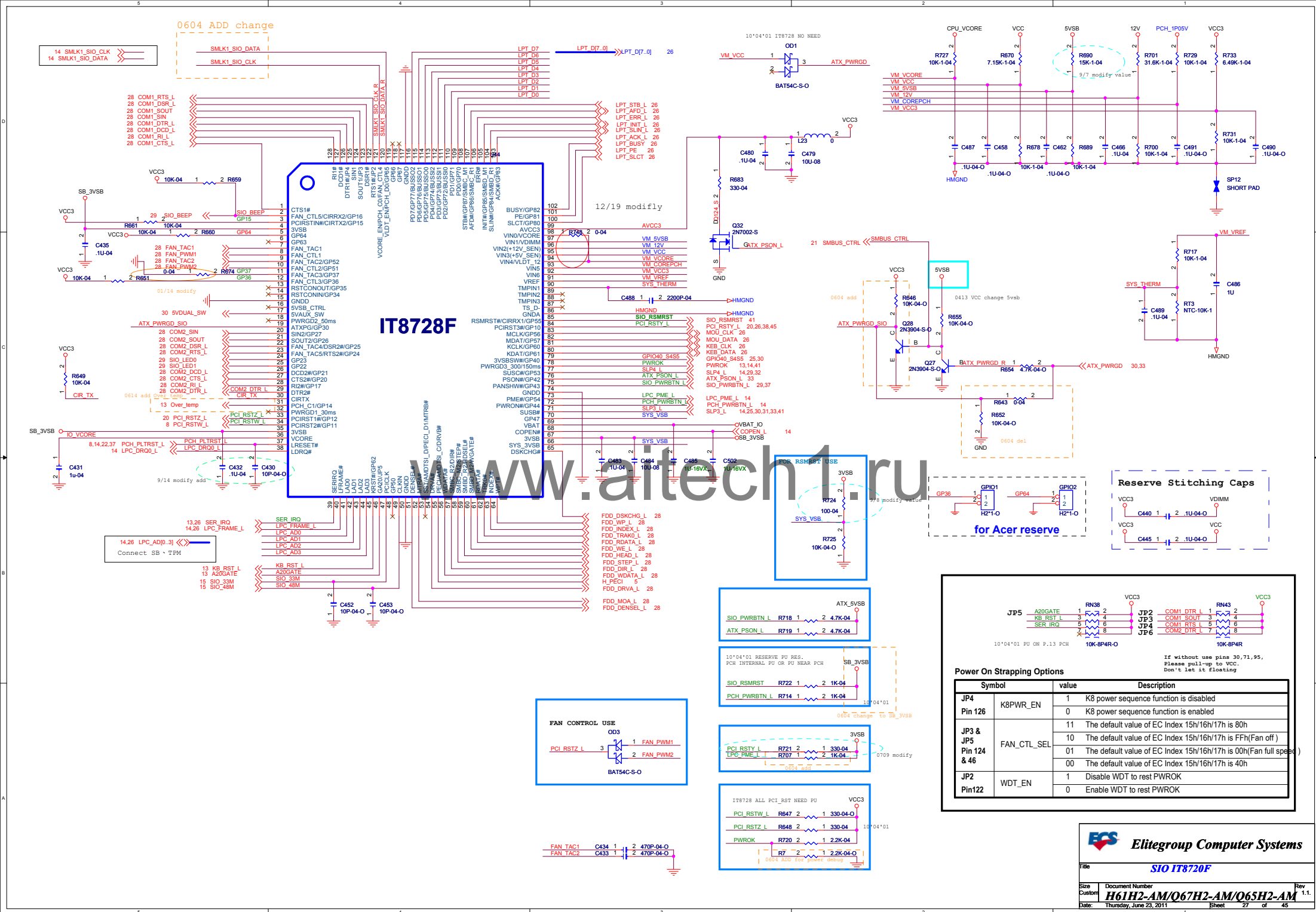
Elitegroup Computer Systems			
AUDIO ALC662 (PANEL)			
Size B	Document Number	Rev	
	H61H2-AM/Q67H2-AM/Q65H2-AM	1.1	
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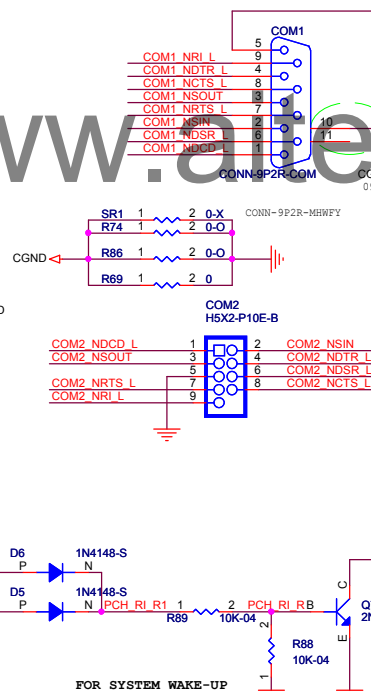


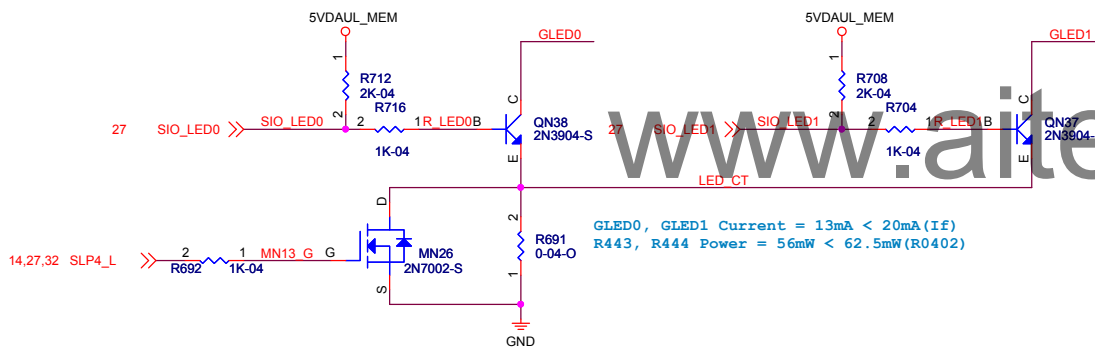
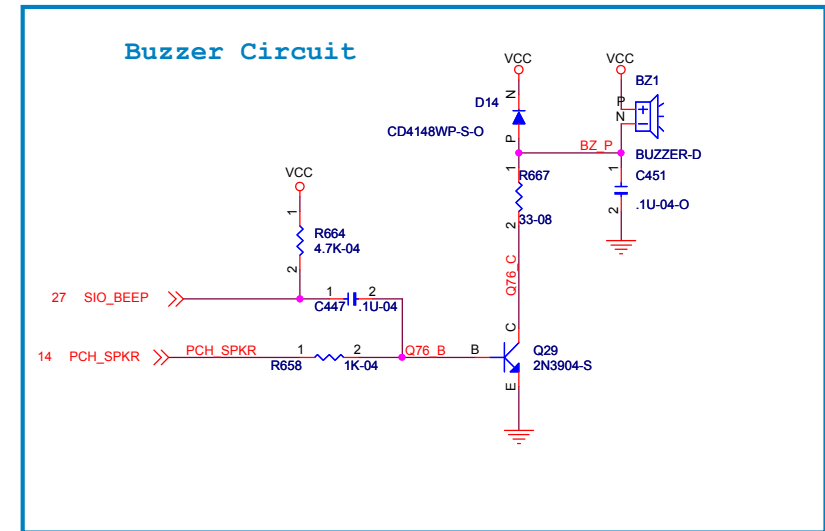
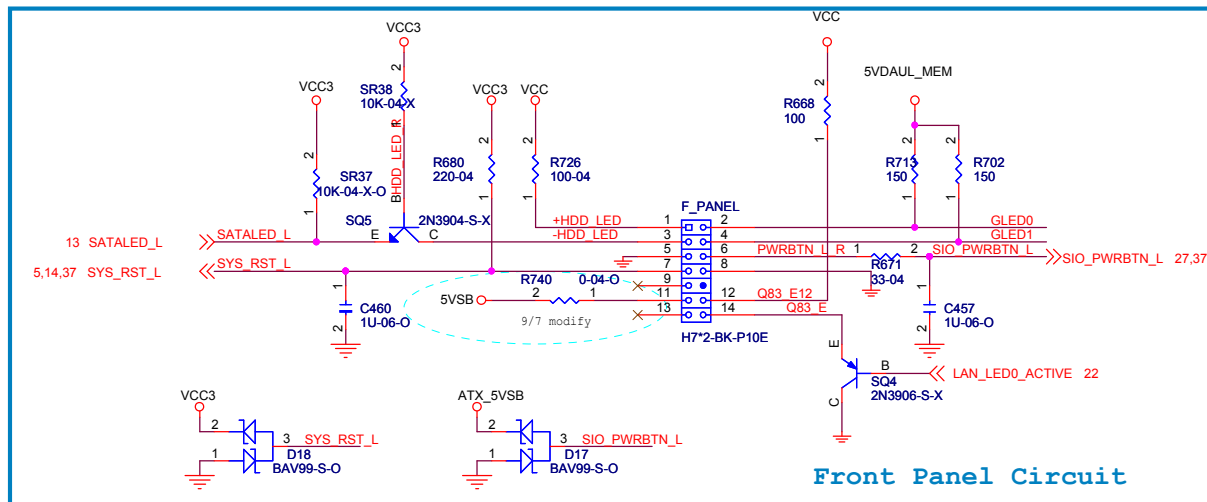
FRONT PANEL USB HEADER

REAR PANEL USB HEADER

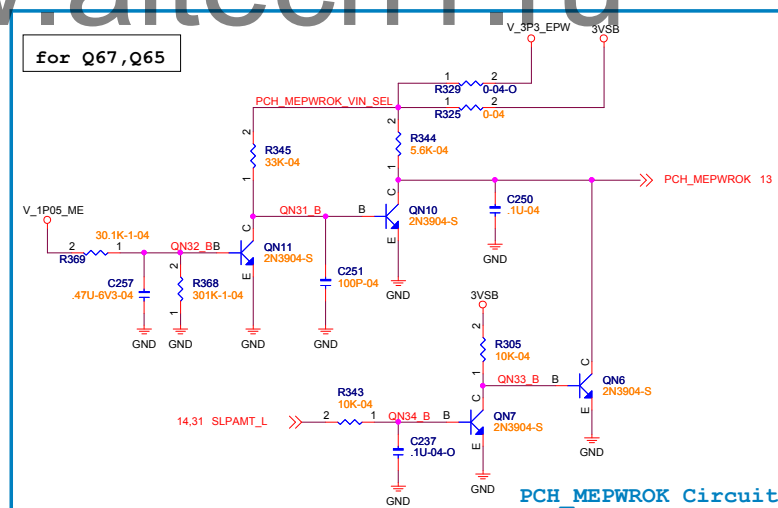
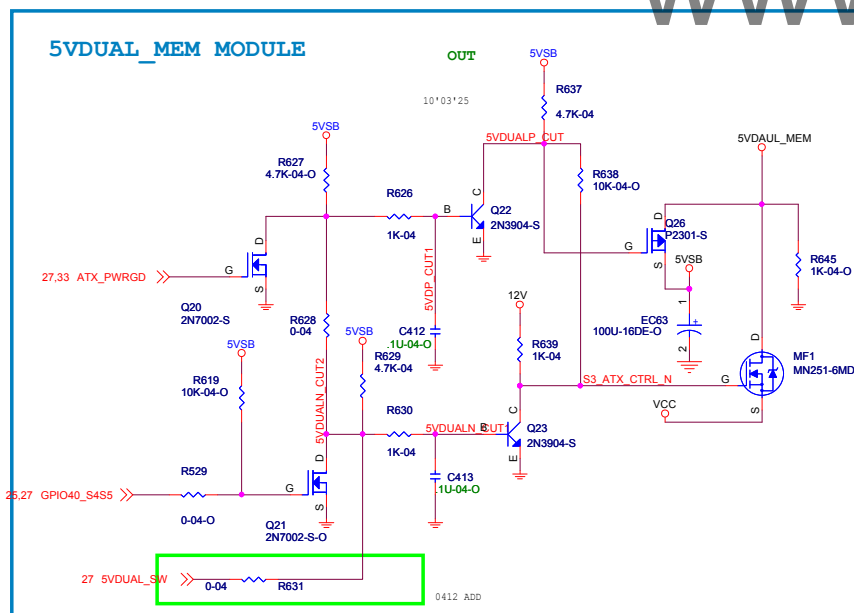
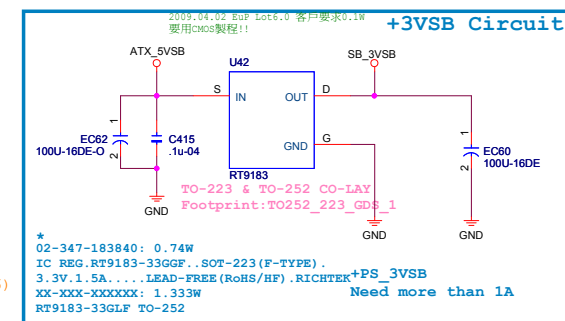
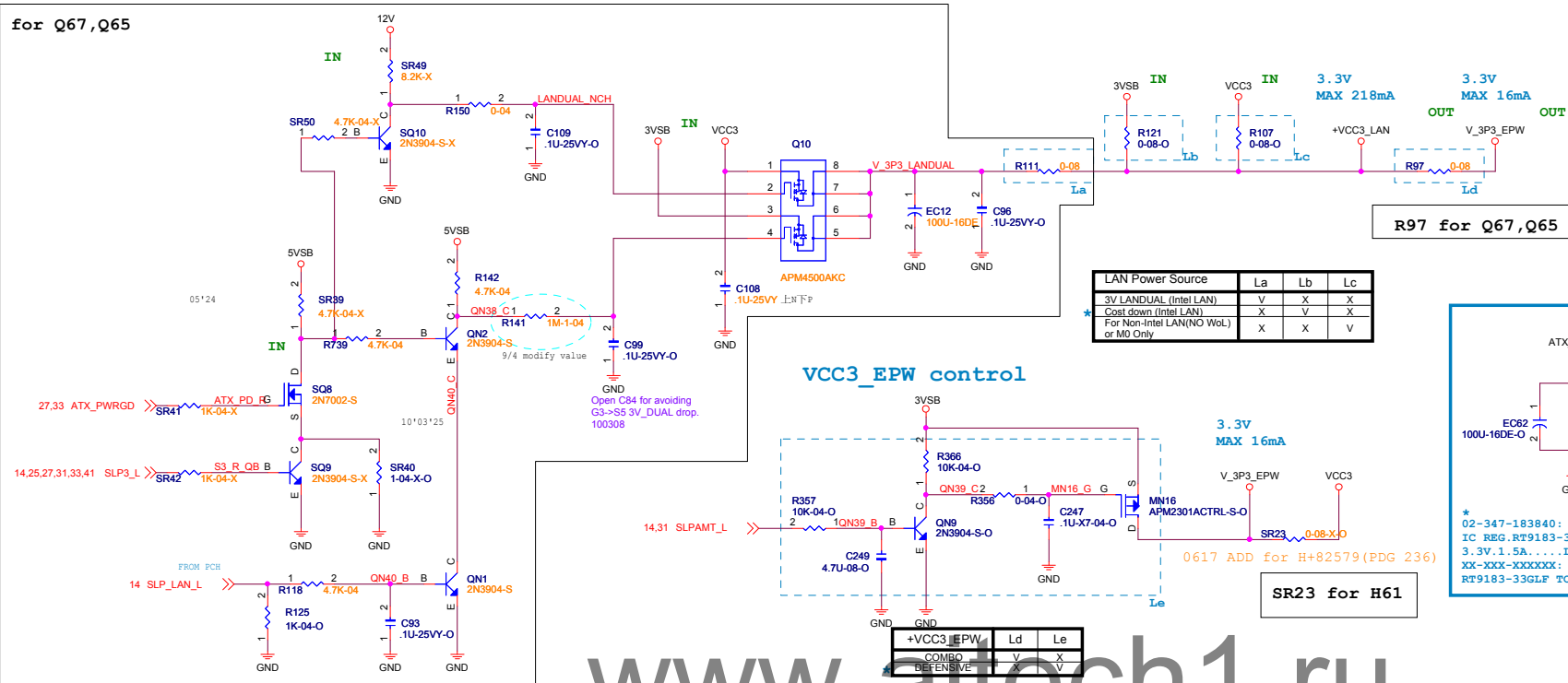


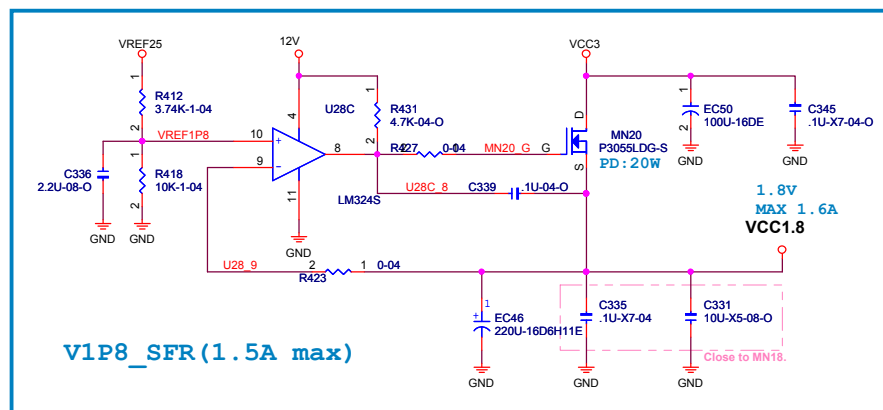
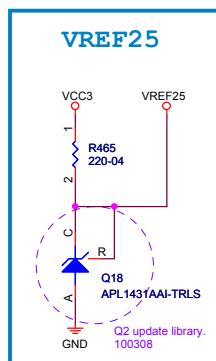
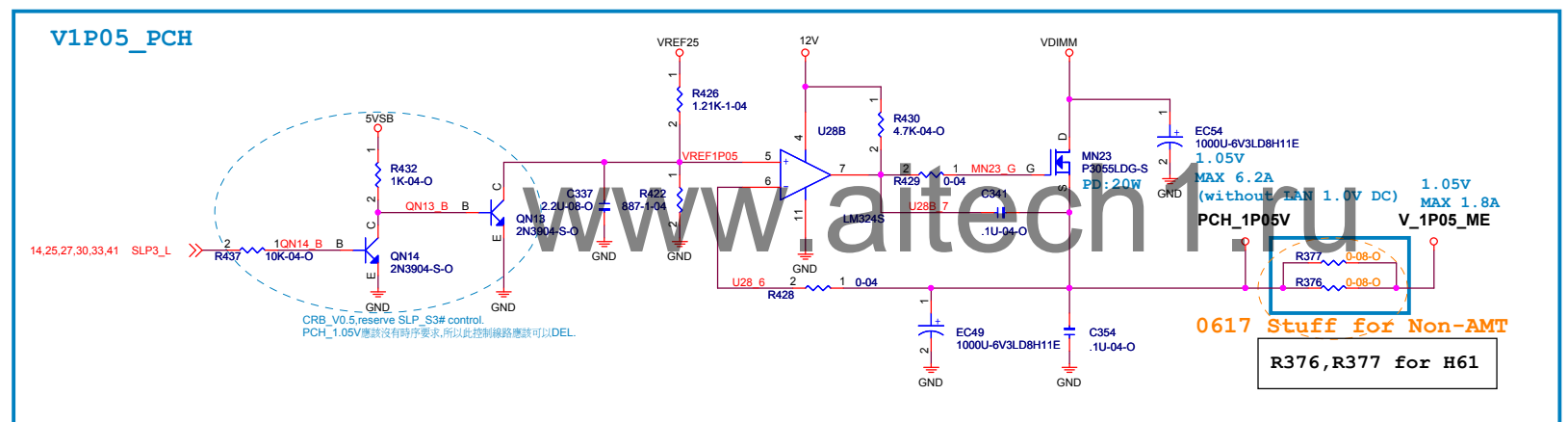
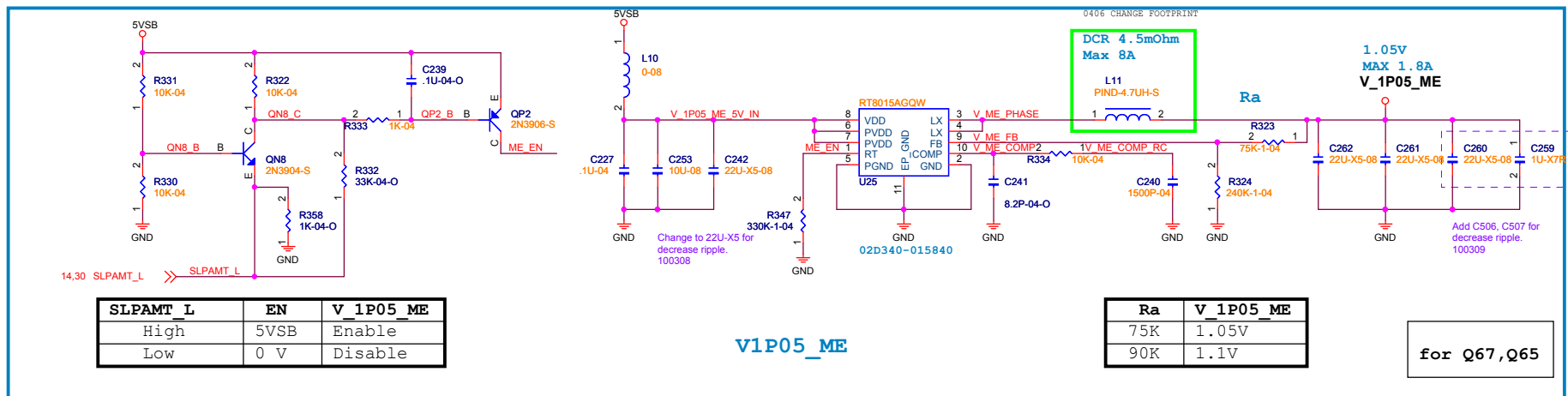






for Q67,Q65





★

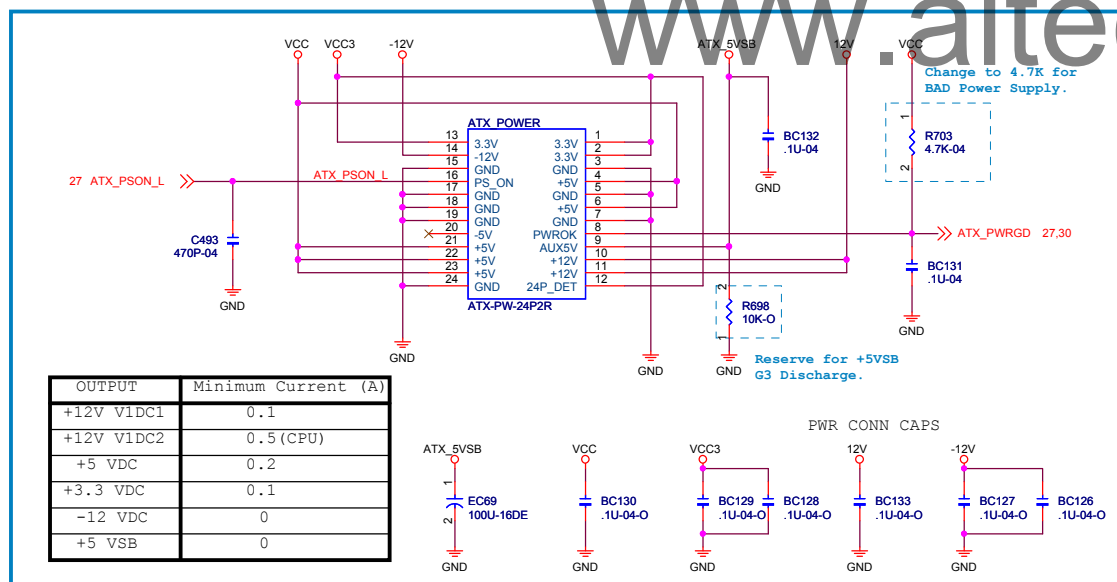
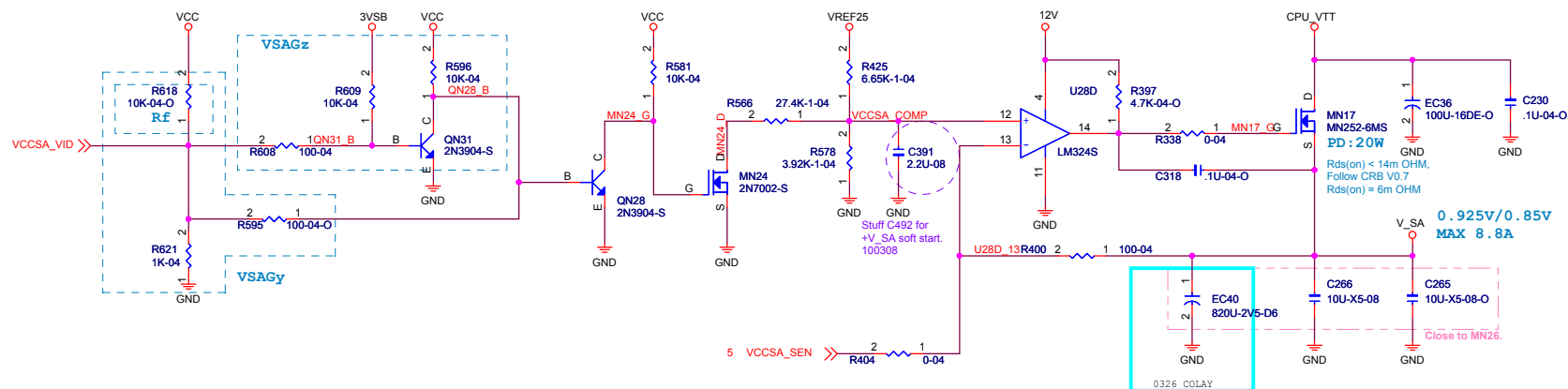
Stuff VSAGz

VCCSA voltage selection	
VID	+V SA
0	0.925V
1	0.85V

VCCSA voltage selection	
VID	+V _{SA}
0	0.925V
1	0.85V

VCCSA voltage selection	
Rf	+V _{SA}
unstuff	0.85V
stuff	0.925V

VCCSA voltage selection	
Rf	+V _{SA}
unstuff	0.85V
stuff	0.925V



ATX Power 24PIN

A Sequence

34 VTT_PWRGD

2 1 R611 10K-04 QN33 B

5VSB

2 1 R598 10K-04 QN30 B

QN33 2N3904-S

QN30 2N3904-S

GND

14,25,27,30,31,41 SLP3_L

2 1 R610 10K-04 QN32 B

5VSB

2 1 R597 10K-04 QN29 B

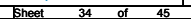
QN32 2N3904-S

QN29 2N3904-S

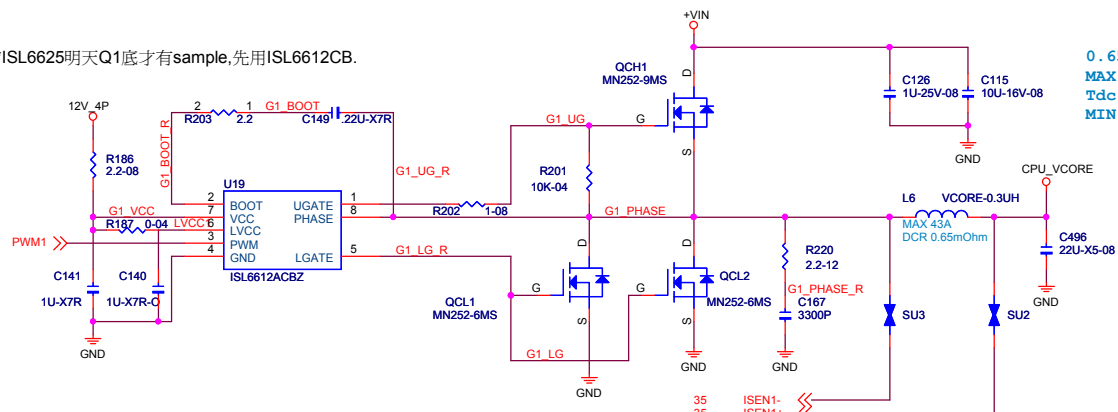
GND

VCC5V_COMP

VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V

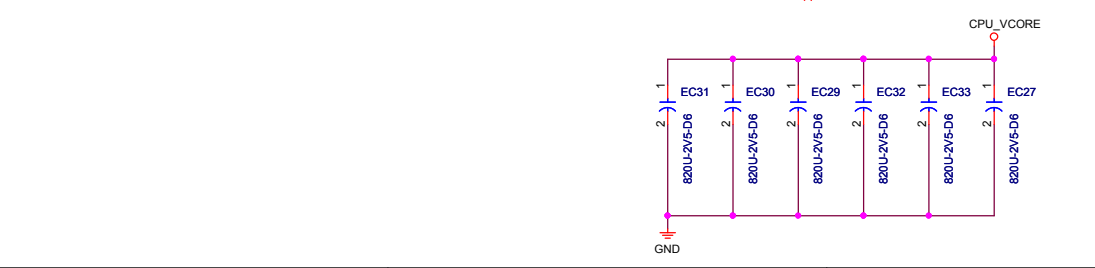
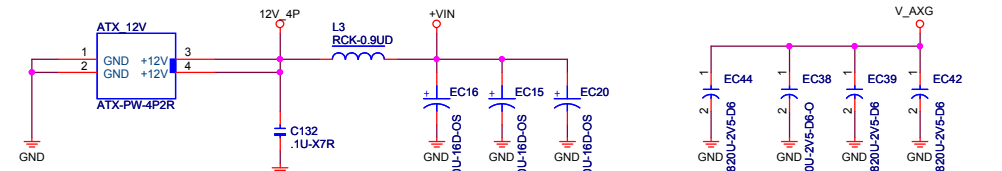
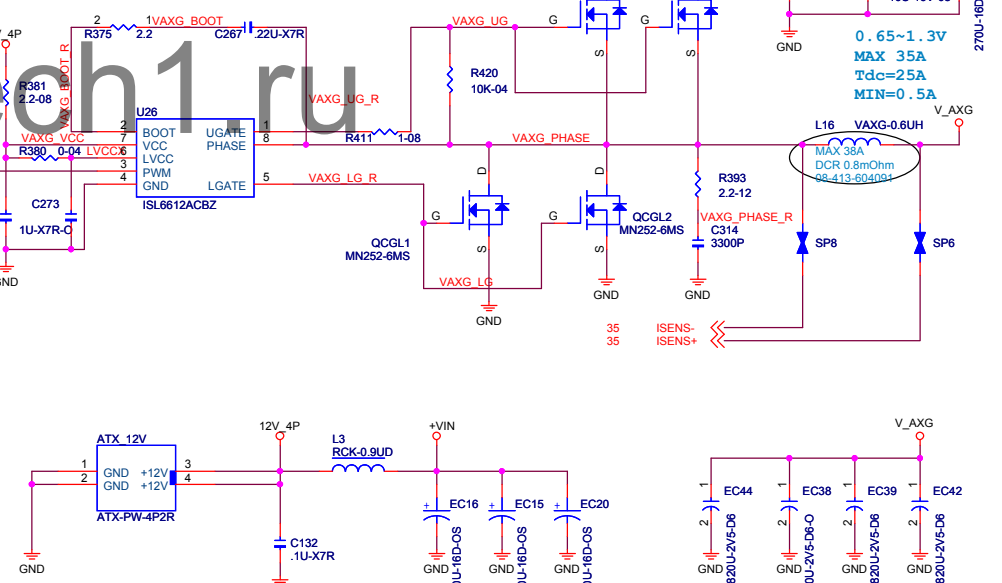
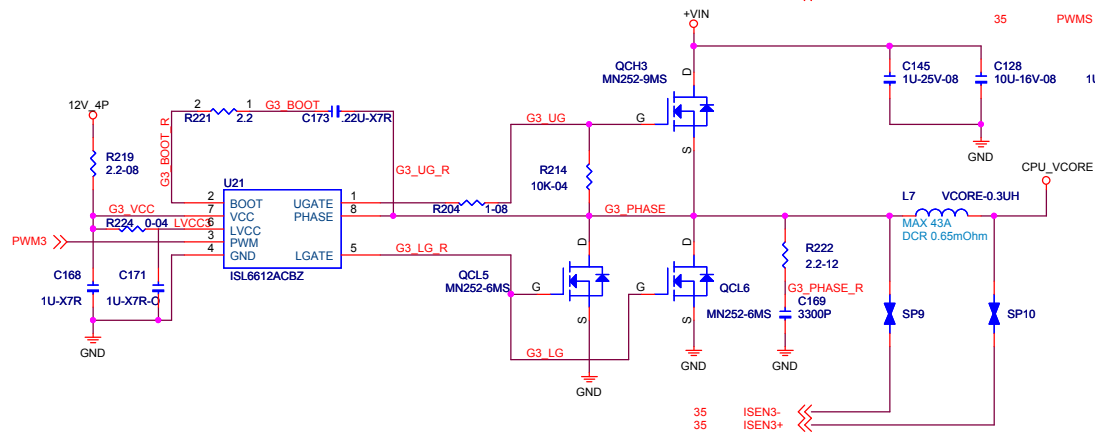
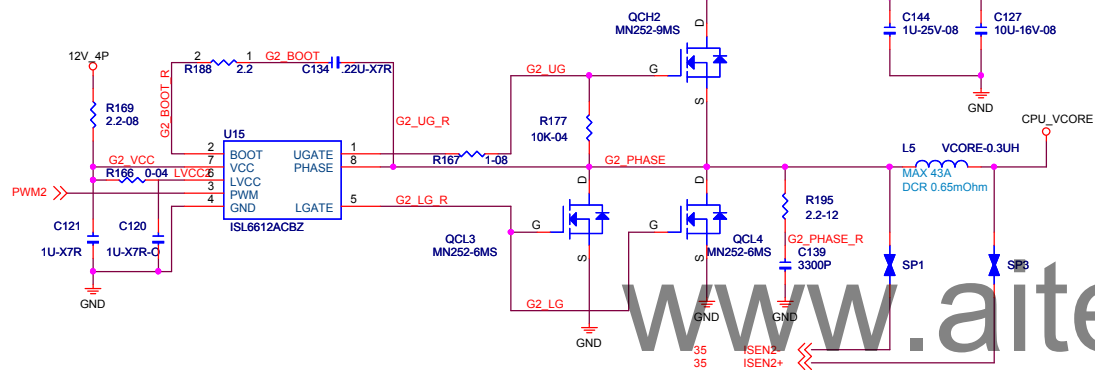


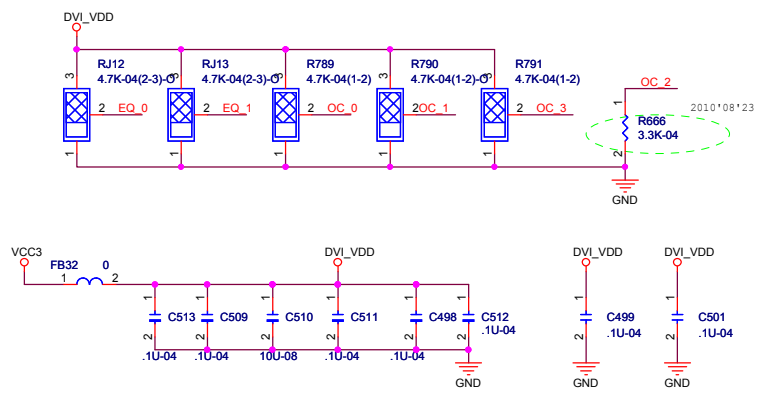
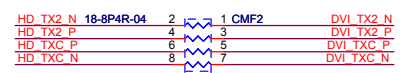
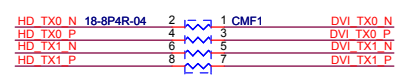
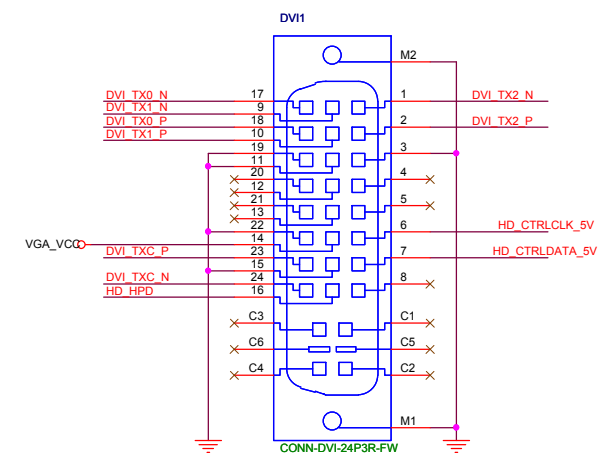
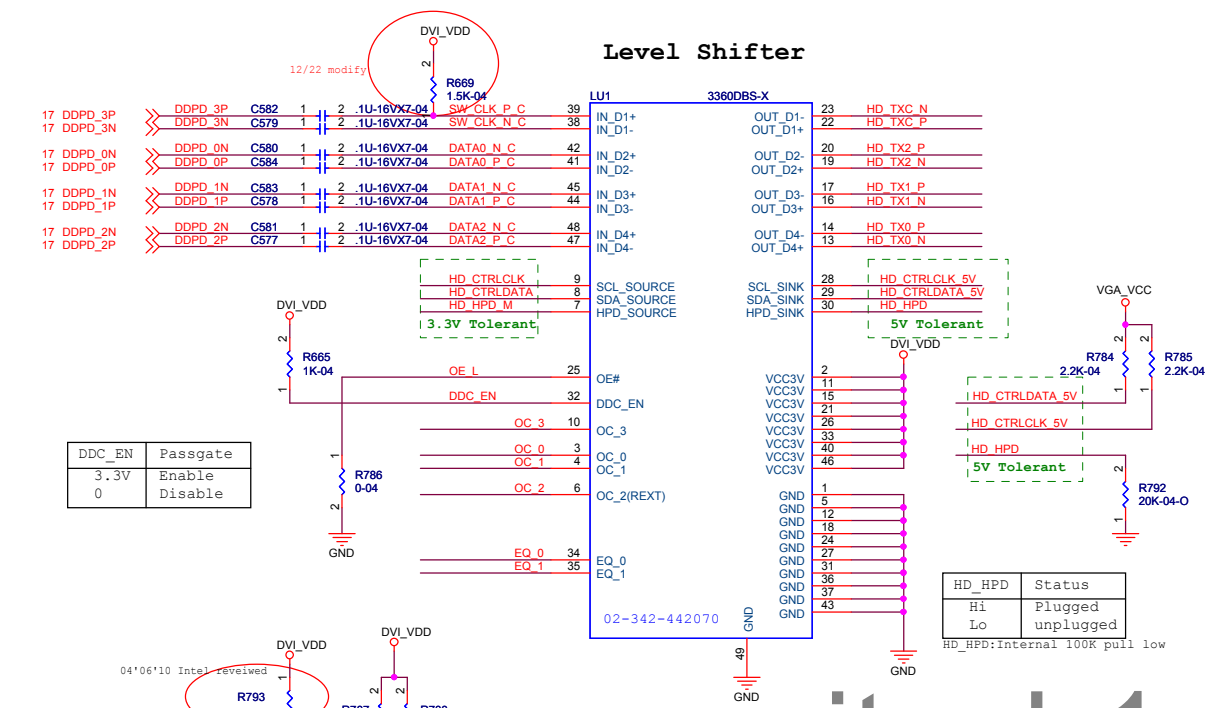
**ISL6625明天Q1底才有sample,先用ISL6612CB.

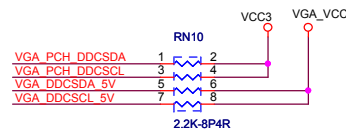
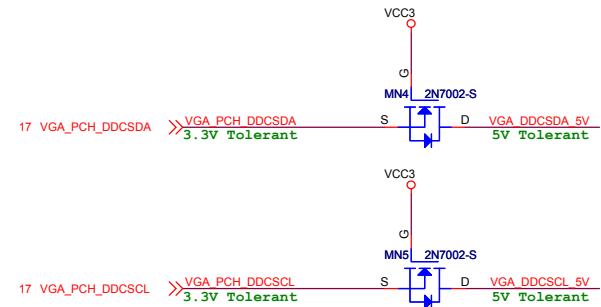
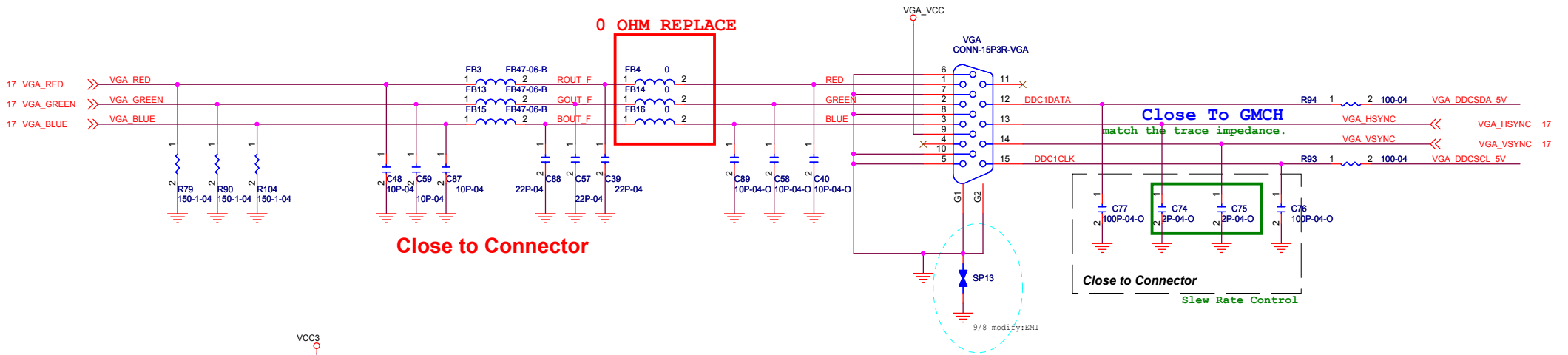


Stuff for ISL6612,
Open for ISL6625.

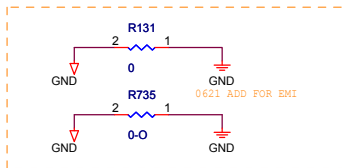
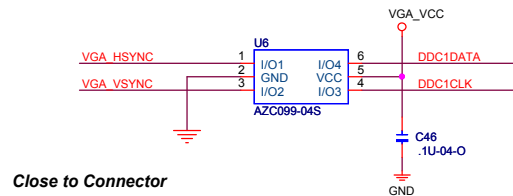
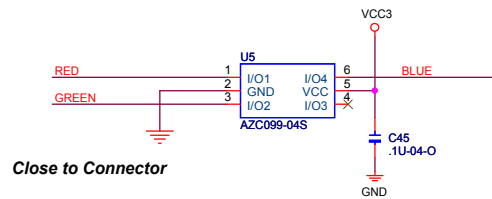
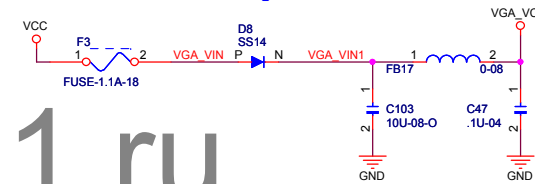
Open for ISL6612,
Stuff for ISL6625.



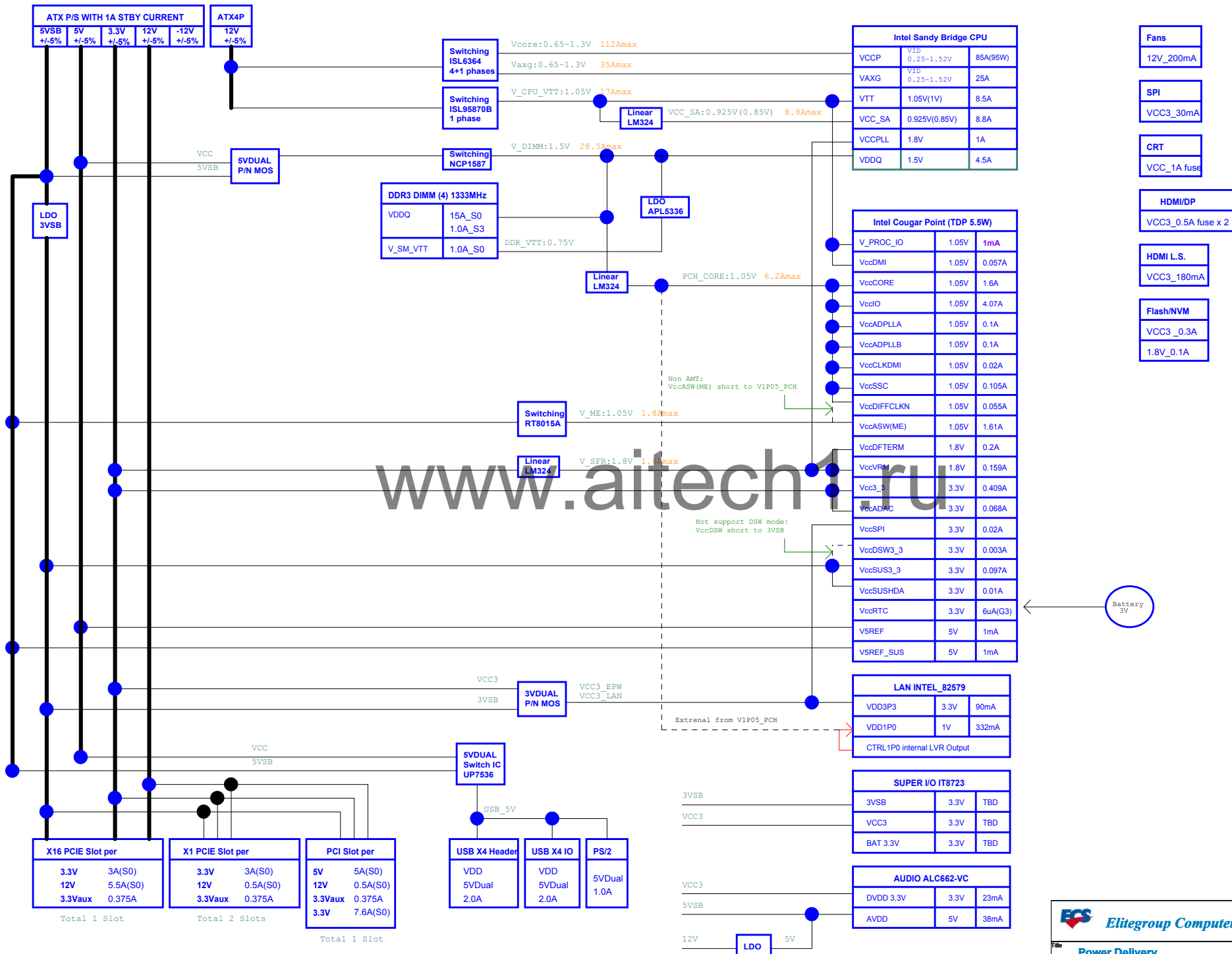


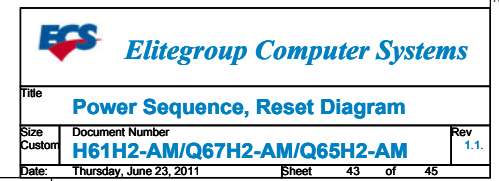


If build in Internal DVI/HDMI Con,
that can use the circuit to protect reverse voltage together.



Elitegroup Computer Systems			
Title			
VGA CONNECTOR			
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Custom	H61H2-AM/Q67H2-AM/Q65H2-AM	1.1.	
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NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

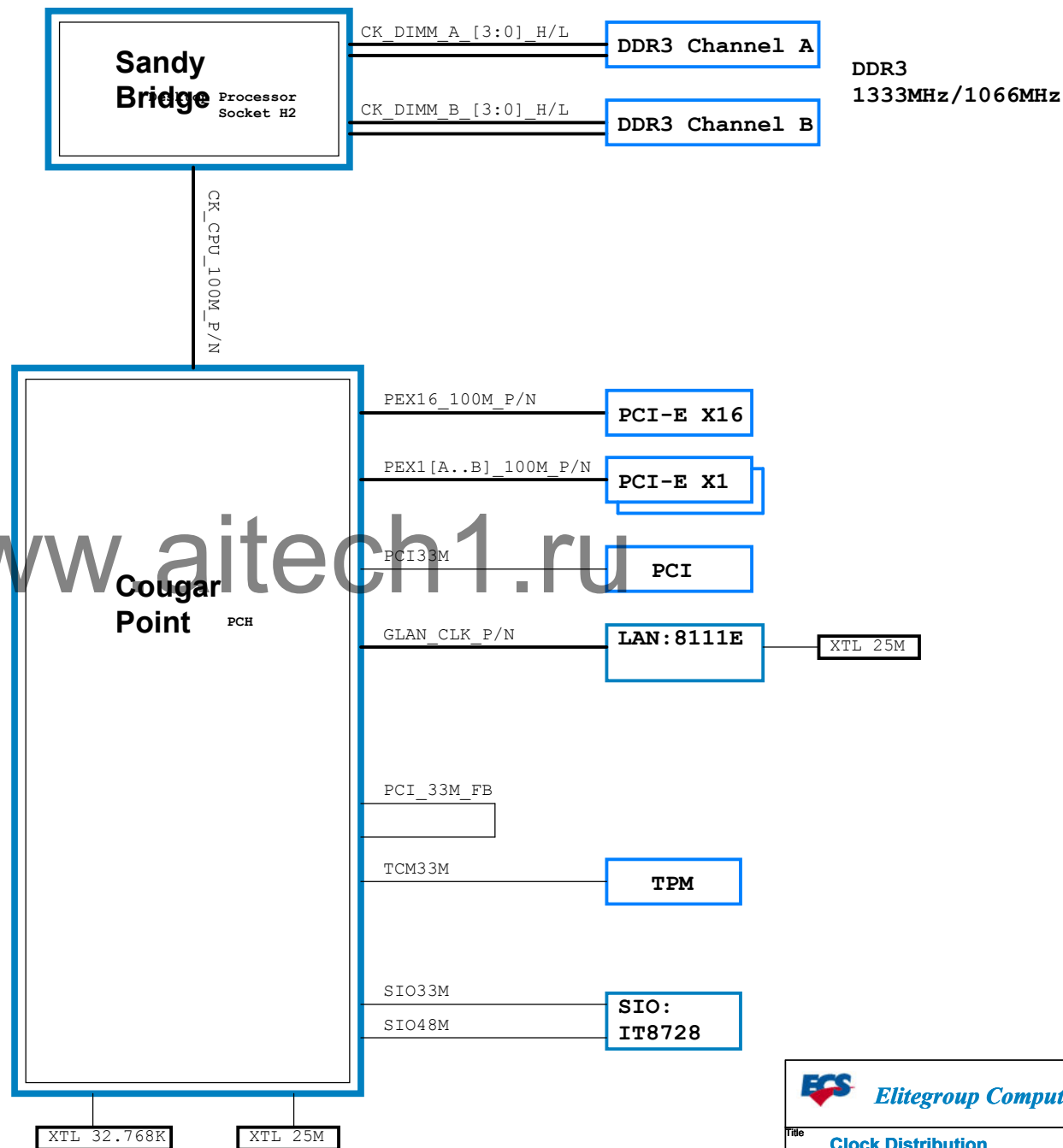
Please refer to

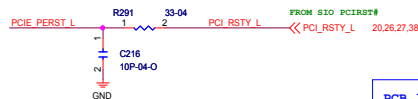
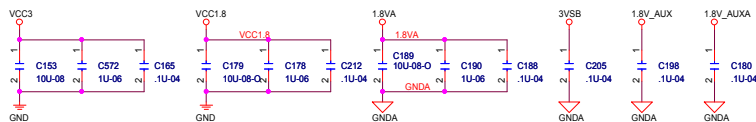
Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

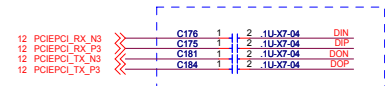
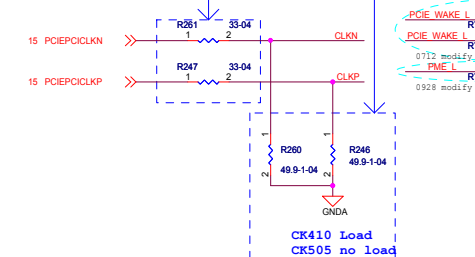
Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG





PCB layout note:
PCIE CLK signals Close to Chip
The termination will only be required on the system board if the resistors are not provided



PCB layout note:
PCIE TX signals
Close to chip

PCIE DIP/DIN/DOP/DON PCB layout note:
To meet Differential Impedance :85 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
PCIE DIP and DIN trace width:9.5 mils
PCIE DOP and DON trace width:9.5 mils
Space between DIP/DIN and DOP/DON:14.5 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 2 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inches (Max.)
The size of C12;C13 is "0402"

PCIE CLK PCB layout note:
To meet Differential Impedance :100 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
CLKP and CLKN trace width:7 mils
Space between CLKP and CLKN:14 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 4 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inches (Max.)
The size of R4;R5 is "0402"
The size of R6;R7 is "0402"

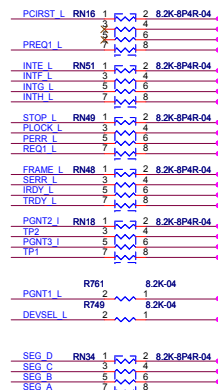
PCB layout note:
Connect to PCIE
PERST# Signal (A11)



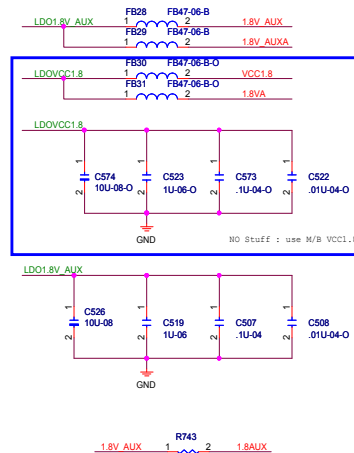
PCB layout note:
Close to chip



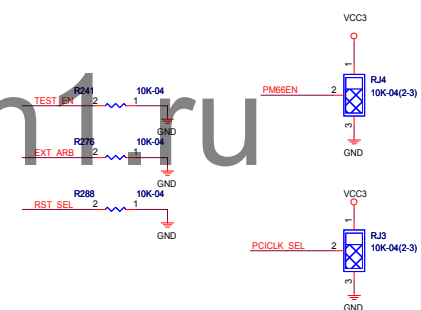
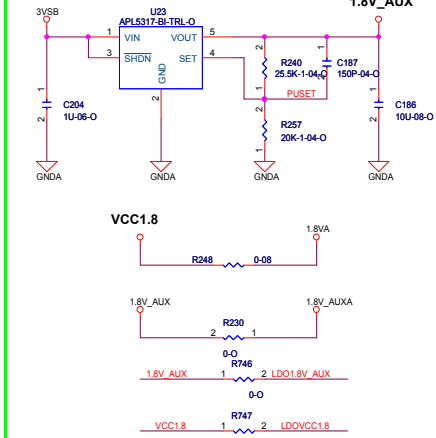
PCI BUS 3.3V external pull up



For BX load



For AX load



1-2: Enable PCI CLK 66MHz
2-3: Disable PCI CLK 66MHz
1-2: PCICLK INPUT form CLK Gen
2-3: PCICLK OUTPUT form IT8893 chip

AD0_31	AD0_31	12.21
C_BE_L[0_3]	C_BE_L[0_3]	12.21
PMGEN	PMGEN	21
FRAME_L	FRAME_L	12.21
RDY_L	RDY_L	12.21
STOP_L	STOP_L	12.21
DEVSEL_L	DEVSEL_L	12.21
PAR	PAR	12.21
SERR_L	SERR_L	12.21
PERR_L	PERR_L	12.21
POrst_L	POrst_L	12.21
PLOCK_L	PLOCK_L	12.21
PCIS3M	PCIS3M	15.21
INTF_L	INTF_L	12.21
INTL_L	INTL_L	12.21
REQ1_L	REQ1_L	12.21
GNT1_L	GNT1_L	12.21
PCIE_WAKE_L	PCIE_WAKE_L	14.20.38

1. 8893 change to PCIE 3
2. USB3,5 change witch USB12,13
3. DP轉HDMI
4. TCP
5. SIO CPU VCORE
6. DVI CLK PULL HIGH
7. LAN colay 8111E VL
8. LEVEL SHIFTER NXP change to ASMT

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<Title>			
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